HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

12606B

DISC MEMORY INTERFACE KIT

Card Assemblies

12606-6001, Rev 845

12606-6002, Rev 902

Note

This manual should be retained with Volume Three
of the HP Computer System Documentation.

12606-90012

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

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SECTION I

GENERAL INFORMATION

1-1. INTROOUCTION.

1-2. This manual provides installation, operating, programming, and service information for the Hewlett-Packard (HP) 12606B Disc Memory Interface Kit.

1-3. DESCRIPTION.

1-4. GENERAL.

1-5. The equipment portion of the kit furnishes the control circuits and cable for connecting an HP 2770A/-001/-002/-003 or 2771A/-001/-002/-003 Disc Memory to an HP 2114B, 2115A, 2116A, or 2116B Computer. The control circuits are on two plug-in cards which install in the computer card cage. The cable supplied with the kit connects the cards to the disc memory.

1-6. The cards must not be installed in the HP 2150A or 2150B Input/Output and Memory Extender, or in the 2151A Input/Output Extender. These extender units do not have the direct memory access capability necessary for operation of the disc system.

1-7. INTERFACE KIT CONTENTS.

1-8. The disc memory interface kit consists of the following:

a. Data channel interface card (part no. 12606-6001).

b. Command channel interface card (part no. 12606-6002).

c. Interface cable, 10 feet (part no. 12606-6004).

d. Disc diagnostic tape (part no. 20346C).

Note

The part number of the program tape includes a suffix letter which identifies a particular revision of the tape. The first issue of a tape is identified by the letter A. Subsequent revisions are identified in alphabetical sequence as B, C, D, etc. If revision of a tape requires changes to associated documentation, an updating supplement for the documentation is supplied when the new tape is furnished. Always use the latest revision of a program tape, even if different from that specified in this manual, together with all updating documentation.

e. Operating and service manual with supplement covering diagnostic program procedures (part no. (12606-90012).

1-9. IDENTIFICATION.

1-10. Hewlett-Packard uses five digits and a letter (00000A) to identify standard interface kits. If the designation of the kit received does not agree with the designation on the title page of this manual, there are differences between the kit received and the kit described in this manual. These differences are explained in change sheets and manual supplements available at HP Sales and Service Offices. (Addresses of these offices are listed at the back of this manual.)

1-11. The two plug-in printed circuit cards supplied with the kit are each identified by a part number marked in a corner of the card. In addition to a part number, each card is further identified by a letter, a date code, and a division code marked on the card (e.g. A-921-22). The letter identifies the version of the etched circuit on the card. The date code (three digits) refers to the electrical characteristics of the board with components mounted. The division code (two digits) identifies the Hewlett-Packard division which manufactured the card. If the date code on a printed-circuit card does not agree with the date code shown on the corresponding logic diagram in this manual, the card differs from the one described in this manual. These differences are explained in change sheets or a manual supplement available at HP Sales and Service Offices.

1-12. The interface cable is identified by its part number, marked on one of the plugs attached to the cable.

1-13. The diagnostic program tape is identified by name and part number, marked on a label affixed to the beginning of the tape.

1-14. The manual and manual supplement are identified by title, part number, and publication date, marked on the title page of the document.

1-15. ADDITIONAL ITEMS REQUIRED.

1-16. EQUIPMENT.

1-17. In addition to the computer, disc memory, and disc memory power supply, use of the disc memory interface kit requires that the computer include the direct memory access (DMA) option. This option consists of the HP 12578A or 12578A-001 Accessory Kit (for the HP 2115A, 2116A, or 2116B Computers), or the HP 12607A Accessory Kit (for the HP 2114B Computer).

1-18. Use of the disc diagnostic tape requires that the computer installation include an HP 2752A or 2754B Teleprinter.

1-19. DOCUMENTS.

1-20. In addition to the manual and manual supplement supplied with the disc memory interface kit, the following documents furnish information pertinent to the use of the interface kit:

a. Operating and service manual for direct memory access kit, manual part no. as follows:

(1) Part no. 12607-90002 for the 12607A Direct Memory Access Kit.

(2) Part no. 12578-9001 for the 12578A or 12578A-001 Direct Memory Access Kit.

b. Operating and service manual for the disc memory, manual part no. as follows:

(1) Part no. 02770-9001 for the 2770A/-001 or 2771A/-001 Disc Memory.

(2) Part no. 02770-90043 for the 2770A-002/-003 or 2771A-002/-003 Disc Memory.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides information for unpacking, initial inspection, installation, and checkout of the disc memory interface kit. The computer, disc memory, disc memory power supply, and other required equipment, should be installed and prepared for operation before installing the interface kit.

2-3. UNPACKING AND INITIAL INSPECTION.

2-4. If the disc memory interface kit is received separated from the computer, inspect the carton containing the kit before opening. If there is external evidence of damage, or if the box rattles, request that the carrier's agent be present when the carton is opened.

2-5. Inspect each component of the kit as the parts are unpacked. Look for such evidence of damage as cracks, dents, broken components, detached parts, corrosion, water damage, etc. If any part of the kit is damaged, retain the carton, packing material, and shipping papers, and immediately notify the carrier and the nearest Hewlett-Packard Sales and Service Office. The Sales and Service Office will arrange for repair or replacement of damaged parts without waiting for settlement of claims against the carrier.

2-6. After inspecting all components, refer to paragraph 1-7 of this manual and ensure that the kit is complete. Also check the part numbers given in paragraph 1-7 against the part numbers on the kit components. If the kit is incomplete, or if an incorrect component has been furnished, notify the nearest Hewlett-Packard Sales and Service Office.

2-7. PREPARATION FOR INSTALLATION.

2-8. COMPUTATION OF CURRENT REQUIREMENTS.

2-9. The cards in the interface kit obtain their operating voltages from the computer power supply. Before installing the cards, it is necessary to determine whether they will impose an excessive added load on the power supply. Together, these cards require 2.40 amperes from the +4.5 volt source, and 0.24 amperes from the -2 volt source. If these amounts will overload the computer power supply, an HP 2160A Power Supply Extender must be used.

2-10. The disc memory has its own power supply, which furnishes all ac and dc operating voltages required by the disc memory.

2-11. PROTECTION OF TRACKS.

2-12. A track protect switch on the data channel interface card permits a read-only status to be selected for some or all disc tracks. This protect feature is in effect when the switch is in the up position. As shipped from the factory, the card can protect track 000 only. By removing diodes from the card before it is installed in the computer, additional groups of tracks can be protected when the switch is in the up position.

2-13. If protection is not desired for any track, no removal of diodes is required. The track protect switch is simply set to the down position when the computer is in operation. Similarly, if only track 000 is to be protected, no diodes are removed, and the track protect switch is set to the up position when track protection is desired.

2-14. When more than one track is to be protected, diodes are removed from the data channel interface card in accordance with table 2-1. If the disc has fewer than 200 (octal) tracks, the table applies to the extent of the number of tracks on the disc.

Table 2-1. Track Protect Diodes

TRACKS PROTECTED WITH TRACK PROTECT SWITCH UP (OCTAL TRACK ADDRESS)	QUANTITY OF PROTECTED TRACKS (DECIMAL)	DIODES REMOVED
00	1	None
00, 01	2	CR1
00 through 03	4	CR1,2
00 through 07	8	CR1,2,3
00 through 17	16	CR1 through CR4
00 through 37	32	CR1 through CR5
00 through 77	64	CR1 through CR6
00 through 177	128	CR1 through CR7

2-15. The locations of track protect diodes are shown in figure 5-2. Diodes which have been removed can later be replaced to reduce the number of tracks protected. When removing or replacing diodes, observe the normal precautions for avoiding damage to components and circuit cards.

2-16. INSTALLATION.

2-17. Installation of the disc memory interface kit is performed as follows:

a. Set the power ON switch on the disc memory power supply to the off (down) position.

b. Remove power from the computer by means of the computer POWER switch.

c. Gain access to the computer card cage, and insert the data channel interface card (part no. 12606-6001) in the card slot corresponding to the desired I/O address and select code.

d. Insert the command channel interface card (part no. 12606-6002) next to the 12606-6001 card. The I/O select code of the 12606-6002 card must be 1 less than that of the 12606-6001 card.

e. Connect the double connector on the end of the interface cable (part no. 12606-6004) to the two interface cards. The portion of the connector marked DATA must fit on the data channel interface card, and the portion marked COMMAND must fit on the command channel interface card.

CAUTION

In the next step, do not accidentally make connection to connector J3 of the disc memory power supply.

f. Connect the 50-pin plug on the interface cable to connector J10 on the disc memory. Leave sufficient slack in the cable to prevent strain.

2-18. INSTALLATION CHECKOUT.

2-19. After installation, check the operation of the disc memory, disc memory power supply, and disc memory interface kit by running the disc memory diagnostic program described in the supplement to this manual. In the read/write portion of the program, check all tracks and sectors on the disc, making at least three passes of the test using the worst-case test word; 1100110011001100CC.

SECTION III

PROGRAMMING

3-1. INTRODUCTION.

3-2. This section contains information for programming the disc memory interface. The following topics are discussed:

a. Disc characteristics.
b. Sector and track addresses.
c. Channel addresses.
d. Timing
e. Parity.
f. Disc status word.
g. Read/write transfer.
h. End-of-track.
i. Multiple disc programming.
j. Track protection.
k. Write or read abort.
l. DMA lockup.
m. Power-off periods.
n. Interrupts.
o. Programming procedure.

3-3. Refer to the operating and service manual for the DMA option for additional programming information.

3-4. DISC CHARACTERISTICS.

3-5. Data is organized on the surface of the disc in bits, words, sectors, and programmable tracks. A programmable track is a track that can be addressed by the program with a given track number. The programmable track is made up of four physical tracks, all associated with the same track number. When writing or reading takes place in a programmable track, circuits in the disc memory automatically select the appropriate physical track. Two disc revolutions are required to write or read an entire programmable track. Each programmable track consists of 90 sectors, each sector being made of of 64 17-bit words. Thus, there are 5760 words in a programmable track.

3-6. As far as programming is concerned, and for explaining the theory of operation of the disc interface cards, the programmable track may be considered a single physical track. Consequently, henceforth in this manual the term "track" will be used when referring to a programmable track.

3-7. The principal programming characteristics of the disc memory are shown in table 3-1.

3-8. SECTOR AND TRACK ADDRESSES.

3-9. The smallest addressable unit of data in the disc memory is one sector (64 words). In each track, the sectors are identified by the octal numbers 000 through 131, proceeding in numerical sequence from the track origin.

3-10. Tracks are identified in octal notation, starting with track number 000 and proceeding in numerical sequence to the highest numbered track.

3-11. CHANNEL ADDRESSES.

3-12. The disc system has a data channel and a command channel, each of which can be addressed by the computer program. The data channel is associated with the data channel interface card, and is addressed by using the I/O select code for that card. The command channel is associated with the command channel interface card, and is addressed by the I/O select code for the command channel card.

3-13. COMMAND CHANNEL I/O SELECT CODE.

3-14. The command channel I/O select code can be used in the OTA/B, LIA/B, CLF, SFS, and SFC instructions. The OTA/B instruction sends to the disc system a control word which specifies the starting track and starting sector for a disc data transfer operation. The control word also

Table 3-1. Disc Memory Characteristics

DISC TYPE	QUANTITY OF TRACKS	TRACK ADDRESS RANGE (OCTAL)	TOTAL NO. OF WORDS
2770A (unexpanded)	32	000-037	184,320
2770A-001/-002/-003	64	000-077	368,640
2771A (unexpanded)	64	000-077	368,640
2771A-001/-002/-003	128	000-177	737,280

NOTE: Numbers in this table are in decimal form unless otherwise specified.

indicates whether reading or writing will take place. The LIA/B instruction acquires a disc status word from the disc system. The CLF and SFS instructions are used principally for equipment diagnostic purposes, and indicate when the track origin is reached or passed. The SFC instruction checks the state of the SCP flip-flop on the disc command card; this instruction is used only for equipment trouble-shooting programming.

3-15. DATA CHANNEL I/O SELECT CODE.

3-16. Two instructions use the data channel I/O select code; these are the STC and CLC instructions. The STC instruction initiates the transfer of data to or from the disc after preliminary instructions have established the disc and core-memory locations to be used. The STC instruction must come after the OTA/B instruction that furnishes the control word containing the disc starting address. However, the time between the OTA/B and STC instructions can be any time that is convenient. The CLC instruction is used to abort a disc read or write operation by cutting off data transfer during the course of the operation.

3-17. TIMING.

3-18. Timing characteristics of the disc are as follows (all figures are approximate because disc speed may vary slightly from the nominal amount):

a. Speed: 3450 RPM for a disc operating from a 60-Hz power line, 2880 RPM for a 50-Hz power line.

b. Maximum access time (time for two disc revolutions): 34.8 milliseconds for the 60-Hz disc, 41.6 milliseconds for the 50-Hz disc.

c. Average access time: 17.4 milliseconds for the 60-Hz disc, 20.8 milliseconds for the 50-Hz disc.

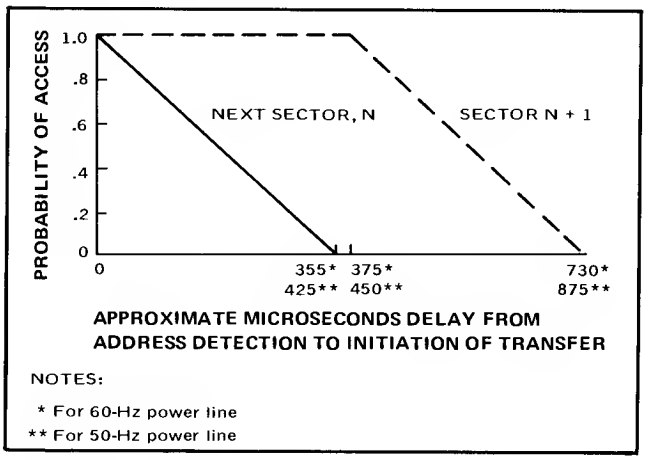
d. Word transfer rate to or from the disc:

(1) For the 60-Hz disc, 6.0 microseconds per word, 375 microseconds per sector, 17.4 milliseconds per 90-sector track (5760 words), 165 words per millisecond.

(2) For the 50-Hz disc, 7.2 microseconds per word, 450 microseconds per sector, 20.8 milliseconds per 90-sector track (5760 words), 135 words per millisecond.

3-19. The address of the next sector to pass under the read/write head forms part of the disc status word. By examining the next-sector address, the program can take action that will most efficiently utilize time. For instance, if disc data are to be read from two groups of sectors, the sectors that will be first to pass under the read/write head can be read first. Another use of the next-sector address is to determine the next sector or sectors available for writing.

3-20. The address indicated for the next sector could immediately precede an address in which reading or writing is desired. However, the time required for execution of read or write instructions may make it impossible to access the desired sector until the following disc revolution. A flag in the disc status word is set to logic 1 when it is impossible to access the next sector in the current disc revolution. When the flag is logic 0, access to the next sector may be possible, depending on how many read or write instructions are required and on how close the sector is to the read/write head. Since there is no indication of the distance of the sector from the read/write head, obtaining access to the sector in the same disc revolution can be expressed only as a probability. Figure 3-1 shows this probability. The horizontal axis of the graph is the time from the end of the LIA/B instruction which acquires the disc status word, to the end of the STC instruction which initiates a transfer of data to or from the disc. Included in figure 3-1 is a line showing the probability of accessing sector N + 1, where N is the next sector. As the illustration shows, the access times are dependent on the power line frequency for which the disc is designed.



2032-1

Figure 3-1. Probability of Sector Access in Current Disc Revolution

3-21. PARITY.

3-22. Each word written on the disc consists of 16 data bits and one parity bit. The parity bit is generated when the word is written, and parity is automatically checked each time the word is read. Occurrence of a parity error is indicated by a flag in the disc status word.

3-23. DISC STATUS WORD.

3-24. The disc status word is a 16-bit word which can be acquired from the disc system by the LIA/B instruction. The instruction must use the disc command channel I/O select code.

3-25. The format and content of the disc status word are shown in table 3-2. The various parts of the word are updated at different times.

3-26. Bits 3 and 1 of the disc status word are reset to logic 0 by an STC instruction with the disc data channel I/O select code. Since this instruction starts a transfer of

Table 3-2. Disc Status Word

BITS	DESCRIPTION
15	Sector Flag. Logic 1 indicates that the sector designated by bits 14-8 of the disc status word is not accessible in the current disc revolution.
14 thru 8	Next-Sector Address. Indicates address of sector which will follow the sector currently under the read/write heads. Bit 8 is the low-order bit.
7	Disc Ready Flag. Logic 1 indicates that the disc is ready for use or is in use. Logic 0 indicates that the disc is currently not ready for use for one of the following reasons: a. Low disc speed. b. Certain disc circuits are defective. c. Disc memory not connected to the computer. d. Disc memory not connected to the disc power supply. e. Low line voltage or no line voltage applied to the disc power supply. f. Disc power supply not turned on or defective.
6	Read Inhibit Flag. Logic 1 when the "not" Read Inhibit signal from the disc is false. Used only for equipment troubleshooting purposes.
5	Sector Address Coincidence Flag. Logic 1 indicates that sector address coincidence has occurred since the last STC instruction addressed the disc data channel. Logic 0 indicates that sector address coincidence has not occurred. This bit is used only for equipment troubleshooting purposes.
4	Not used.
3	Abort Flag. Logic 1 indicates that bit 7 of the disc status word has been logic 0 at least once since performance of the last STC instruction that addressed the disc data channel. Consequently, the data transfer concerned may not have been successfully completed. Logic 0 indicates that bit 7 has been logic 1 since the last STC instruction which addressed the disc data channel. Bit 3 is also set to logic 1 if low AC line voltage is furnished to the disc memory power supply. Bit 3 is reset by an STC instruction that addresses the disc data channel.
2	Writing Enabled Flag. Logic 1 indicates that the currently selected disc track is not protected by the track protect switch. Logic 0 indicates the track is protected. This bit has significance only after a disc track has been specified for writing by an OTA/B instruction.
1	Parity Error Flag. Logic 1 indicates read parity error has occurred. Logic 0 indicates no read parity error has occurred. Bit 1 is reset by an STC instruction that addresses the disc data channel.
0	Disc Busy Flag. Logic 1 indicates that a disc read or write operation has been initiated, is in progress, or is being terminated. Logic 0 indicates that none of these conditions exists. If writing or reading ends before the end of a sector, the busy flag remains logic 1 until the end of the sector is reached.

data to or from the disc, a check of bits 3 and 1 after completion of the data transfer provides an indication of certain types of data transfer failure.

3-27. READ/WRITE TRANSFER.

3-28. At least one sector must be allowed to elapse between the end of a read or write operation and the start of another read or write operation. This precaution must be observed because there is insufficient time between sectors to program the second operation. If an attempt is made to perform such an operation, the first operation will either be aborted before the transfer of all data, or the second operation will wait until rotation of the disc brings the desired sector around for the second time.

3-29. END-OF-TRACK.

3-30. When the end of a 90-sector track is reached while writing or reading, the operation does not continue in the next track. Moreover, a single write or read operation must not cross the track origin; otherwise, at the start of the new track, writing or reading will take place starting at sector 46 (decimal) of the old track. When it is necessary to cross the track origin, a new disc operation must be initiated after the last sector of the track. As a result, two disc revolutions will elapse before the writing or reading will recommence. However, if programmed to do so, the new operation can commence in sector 001 with the loss of only a single sector time.

3-31. MULTIPLE DISC PROGRAMMING.

3-32. When a computer utilizes two or more discs, programming procedures require only that the appropriate command channel and data channel I/O select codes be used for each disc.

3-33. TRACK PROTECTION.

3-34. To write on a protected track, the track protect switch is set to the down (nonprotect) position. The switch is returned to the up (protect) position to re-establish the protect status.

3-35. WRITE OR READ ABORT.

3-36. A disc write or read abort can be initiated by programmed means, or it can be the result of certain types of equipment failure. When an abort occurs, no further data is transferred to or from the disc. If the abort takes place after initiation of a disc operation, but before the first desired sector is reached on the disc, no data is transferred. If fewer than 64 words are programmed to be written or read in the last sector, and an abort of either type occurs after the last desired word has been transferred to or from the disc, the data write or read operation is completed successfully.

3-37. An equipment-failure abort occurs when certain types of fault occur in the disc system. In some cases, when an abort of this type takes place bit 3 of the disc status word is set to logic 1. (Refer to table 3-2.)

3-38. Note that bit 3 of the status word can become logic 1 if an equipment failure occurs after completion of the data transfer operation. Therefore, the bit should be checked as soon as possible after completion of data transfer to or from the disc. Completion of transfer can be determined by an examination of the disc busy bit (bit 0) of the status word. If the disc is still busy, the LIA/B instruction which acquires the status word does not interfere with the transfer of data to or from the disc.

3-39. A programmed abort is brought about by a CLC instruction that addresses the data channel, or which has an I/O select code of zero. A programmed abort also occurs if an OTA/B instruction address the command channel. (Such an OTA/B instruction usually is performed in order to start another disc read or write operation.)

3-40. DMA LOCKUP.

3-41. If a disc write or read operation is aborted as a result of an equipment failure, the DMA system will lock up. When this situation occurs, DMA waits to transfer more words to or from the disc, but the disc system does not send a signal to DMA to indicate that another word is required (when writing) or is ready (when reading).

3-42. It should be noted that a programmed abort, using a CLC instruction with the disc data channel I/O select code or with a zero I/O select code, does not cause DMA lockup.

3-43. When DMA lockup has occurred, a programmed check of the DMA channel, using an SFS or SFC instruction with the DMA channel I/O select code, will indicate that the DMA channel is busy. Futhermore, a check of the disc busy bit (bit 0) of the disc status word will indicate that the disc is busy.

3-44. The lockup condition continues until one of the following actions is performed:

a. Clear the entire I/O system by programming a CLC instruction with a zero I/O select code.

b. Start a new disc write or read operation on the same DMA channel, using the normal disc and DMA initiation instructions. (The 2114B Computer has only a single DMA channel.)

c. Perform a CLF instruction with the DMA channel I/O select code, and a CLC instruction with the disc data channel I/O select code. These two instructions can be programmed in any sequence.

d. Stop the program, then press the PRESET switch.

e. Turn off computer power, then restore power.

3-45. Existence of DMA lockup is indicated by bit 3 of the disc status word. (Refer to table 3-2.) If this bit is logic 1 after sufficient time for completion of the data transfer, an equipment-failure abort has occurred. Another method of checking for an equipment-failure abort is to perform an LIA/B instruction with the DMA channel I/O select code. If sufficient time has been allowed for completion of the transfer, the word count should be zero.

3-46. Checking for an abort condition as described in the preceding paragraph will not interfere with the data transfer operation, if it is still in progress. The check should be made as soon as possible after completion of the transfer of data. This will avoid the possibility of an equipment failure setting the abort flag after completion of the data transfer, thereby erroneously indicating that the transfer was not completed.

3-47. If the computer has two DMA channels, the channel not used for the disc write or read operation is not affected by a DMA channel lockup.

3-48. POWER-OFF PERIODS.

3-49. If ac power is removed from the computer or the disc memory power supply and then restored, data recorded on the disc is retained. However, if disc writing is taking place at the time of power removal, erroneous data may be recorded in the sector in which writing is taking place. If power is removed from the disc memory power supply but not from the computer, the disc ready flag (bit 7 of the disc status word) is logic 0 during the power-off period. Also, the abort flag (bit 3 of the status word) becomes logic 1, and it remains 1 after restoration of disc power. When power is restored to the disc after a

power failure, disc rotation starts without manual intervention. From a stationary start, the disc reaches operational speed in approximately 3 minutes. Bit 7 of the disc status word becomes logic 1 when the disc is up to operating speed.

3-50. INTERRUPTS.

3-51. The disc system does not furnish or receive program interrupts.

3-52. PROGRAMMING PROCEDURE.

3-53. DATA TRANSFER.

3-54. Transfers of data to and from the disc memory are controlled by the DMA system of the computer. The DMA system transfers the disc data to or from the core memory in the computer, suspending the computer program one machine cycle for every 16-bit word transferred. (One machine cycle requires 2.0 microseconds for the 2114B or 2115A Computer, 1.6 microseconds for 2116A or 2116B Computer.) The rate of transfer is determined by the rate at which the disc memory can furnish or receive data.

3-55. The DMA system can transfer up to 16,384 words with one initializing subroutine. One sector is the minimum addressable data unit in the disc memory; however, as few as 2 words can be written in the sector. These words will appear in the first two word locations of the sector addressed. The remainder of the sector will contain the same word that was written in the second word location. Similarly, if more than one sector is written, the last sector can contain from 2 to 64 words. If the last sector contains fewer than 64 words, the last word written is repeated on the disc for the remainder of the sector. Thus any number of words up to 16,384 can be written with a single initialization, with the exception of 1 modulo 64 words. (That is, any number of words up to 16,384 can be written, with the exception of 1 plus any multiple of 64.) If writing of 1 word is programmed, the word will not be transferred to the disc. Similarly, if writing of 1 modulo 64 words is programmed, the last word will not be transferred to the disc. When reading is performed, any number of words from 1 through 16,384 can be read with a single initialization.

3-56. In the read or write subroutine the particular use made of the disc status word is determined by the type of operation being performed, the program time available, and the amount of core storage that can be allocated to the program. Therefore, no concrete rules can be laid down regarding use of the disc status word.

3-57. Normally, the first step in a disc read or write subroutine is to acquire the current disc status word with an LIA/B instruction addressed to the command card. Bits 7 and 0 are then checked to ensure that the disc can be used (refer to table 3-2). Bits 15 and 14 through 8 are also checked if the address of the next sector is pertinent to the operation being programmed.

3-58. After appropriate portions of the disc status word have been checked, initialization of a disc operation follows the procedures used with DMA data transfers. (Refer to the operating and service manual for the DMA option.) In the initialization procedure, four 16-bit control words are used. These are referred to as CW1, CW2, CW3, and CW4. Through the use of the OTA/B instruction the first three of these are forwarded to the DMA system, and the last is furnished to the disc command channel. Table 3-3 describes each of the control words.

Table 3-3. Data-Transfer Control Words

CONTROL WORD	DESCRIPTION
CW1	CW1 is the DMA program control word. Format and content are as follows: Bit 15. If logic 1, turn on the disc control bit flip-flop (perform the function of an STC instruction) after each word is transferred to or from the disc. If logic 0, do not turn on the disc control flip-flop after each word. Bit 14. This bit specifies whether DMA will handle 8-bit bytes or 16-bit words. Since the disc memory stores 16-bit words, bit 14 must be logic 0 for disc data transfers. Bit 13. If logic 1, turn off the disc control bit flip-flop (perform the function of a CLC instruction) after the last disc word has been transferred. If logic 0, do not turn off the disc control bit flip-flop after the last word. Bits 12 thru 6. Not used. Bits 5 thru 0. Disc data channel I/O select code. Bit 0 is the low-order bit.
CW2	CW2 is the DMA memory address register word. Format and content are as follows: Bit 15. Logic 1 specifies core memory write. Logic 0 specifies core memory read. Bit 14 thru 0. Core memory starting address. Bit 0 is the low-order bit.

Table 3-3. Data-Transfer Control Words (Continued)

CONTROL WORD	DESCRIPTION
CW3	CW3 is the DMA block length word. Format and content are as follows: Bits 15 and 14. Not used. Bits 13 thru 0. The 2's complement of the number of words to be transferred to or from the disc. Bit 0 is the low-order bit.
CW4	CW4 is the disc function and disc address word. Format and content are as follows: Bit 15. Logic 1 specifies disc write. Logic 0 specifies disc read. Bit 14. Not used. Bits 13 thru 7. Disc starting track. Bit 7 is the low-order bit. Bits 6 thru 0. Disc starting sector. Bit 0 is the low-order bit.

Table 3-4. Typical Disc Subroutine

OP CODE	OPERAND	REMARKS
		INITIALIZE DMA CHANNEL 1
LDA	CW1	Fetch CW1 from core memory and load in the A-register.
OTA	6	Output CW1 to DMA channel 1.
CLC	2	Prepare DMA channel 1 memory address register to receive CW2.
LDA	CW2	Fetch CW2 from core memory and load in the A-register.
OTA	2	Output CW2 to DMA channel 1.
STC	2	Prepare DMA channel 1 word-count register to receive CW3.
LDA	CW3	Fetch CW3 from core memory and load in the A-register.
OTA	2	Output CW3 to DMA channel 1.
		INITIALIZE DISC MEMORY
LDA	CW4	Fetch CW4 from core memory and load in the A-register.
OTA	11	Output CW4 to disc command channel.
		START TRANSFER OF DATA
STC	6,C	Activate DMA channel 1.
STC	10	Initiate disc data transfer.

3-59. If a disc write operation is to be performed, the disc status word can be read a second time after the disc track is specified by a SW4 word, and bit 2 of the status word can then be checked to ensure that the track is not protected. It is particularly desirable to check bit 2 when the track-protect switch must be set to the nonprotect position in order to write in the selected track. After completion of the data transfer to or from the disc, the disc status word can be read once more to check bit 3. If this bit is logic 1, the data transfer was probably not completed successfully. After a read operation bit 1 can also be checked to determine whether a parity error occurred.

3-60. To demonstrate the principles of disc programming, table 3-4 presents a typical disc subroutine. For simplicity, the subroutine makes no checks of the disc status word. The subroutine reads a block of 4096 (decimal) words in disc track 10 (octal), starting at sector 25 (octal), and stores the words in core memory starting with address 10,000 (octal). DMA channel 1 is used, and the disc interface cards are in slots having an I/O select code of 10 (data channel card) and 11 (command channel card). The control words are as follows:

a. CW1: 020010 (octal). This control word turns off the disc control bit flip-flop after the last word has been transferred (bit 13 is logic 1), and specifies the I/O select code of the disc data channel (bits 5 through 0 are 10, octal).

b. CW2: 110000 (octal). This control word specifies a core memory write operation (bit 15 is logic 1) and designates the starting address in core memory (bits 14 through 0 are 10000, octal).

c. CW3: -4096 (decimal). This control word, after program assembly, specifies the 2's complement of the number of words to be transferred.

d. CW4: 000425 (octal). This control word specifies drum read (bit 15 is logic 0), track 10 (bits 13 through 7 are 010 octal) beginning with sector 025 (bits 6 through 0 are 025, octal).

3-61. TRACK ORIGIN DETECTION.

3-62. To determine when the disc has reached or passed the track origin, first a CLF instruction is performed. This instruction uses the I/O select code of the disc command channel. Then an SFS instruction is performed; this instruction is also addressed to the disc command channel. If the track origin has been passed since performance of the CLF instruction, a program skip occurs. If the track origin has not been reached, the SFS instruction can be repeated as often as suits requirements, until the track origin is reached.

3-63. The track origin check does not interfere with a disc data-transfer operation, if one is taking place.

3-64. SCP FLIP-FLOP CHECK.

3-65. As a computer trouble-shooting procedure, a check can be made of the SCP flip-flop, situated on the command channel interface card. To make this check, an SFC instruction is addressed to the disc command channel. If the SCP flip-flop is clear, a program skip takes place. If the flip-flop is in the set state, no skip occurs.

3-66. Performance of the SCP flip-flop check does not interfere with a disc data transfer operation, if one is taking place.

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section explains the circuit theory of the data channel interface card and the command channel interface card. Operations of the disc memory and computer are described only to the extent required for explaining the functioning of the two interface cards.

4-3. For brevity, the names of equipment items mentioned in this section have been shortened as follows:

a. The HP 12606-6001 Data Channel Interface card is referred to as the "data card".

b. The HP 12606-6002 Command Channel Interface card is referred to as the "command card".

c. The HP 2770A/-001/-002/-003 or 2771A/-001/-002/-003 Disc Memory is referred to as the "disc memory" or "disc".

d. The HP 2772A or 2772A-02 Disc Memory Power Supply is referred to as the "disc power supply".

e. The HP 2114B, 2115A, 2116A, or 2116B Computer is referred to as the "computer".

f. The HP 12578A, 12578A-01, or 12607A Direct Memory Access is referred to as "DMA" or the "DMA system".

4-4. OVERALL FUNCTIONAL DESCRIPTION.

4-5. The data card and command card, under control of the computer, perform the following functions:

a. Determine when the first disc sector of a read or write operation reaches the disc read/write head.

b. When writing on the disc, receive 16-bit parallel words from the computer, generate a parity bit (odd parity is used), and forward the resulting 17-bit word to the disc in serial fashion.

c. When reading from the disc, receive 17-bit serial words from the disc, check parity, and forward the 16 data bits in parallel to the computer.

d. Prevent writing on protected tracks.

e. Forward a disc status word to the computer.

4-6. Interface circuits for controlling the transfer of data to and from the disc are situated principally on the command card. Additional control circuits are located on the data card, together with circuits for handling the data transferred.

4-7. The DMA system transfers to or from the computer all words written on the disc or read from the disc. DMA and the disc memory conduct these operations without the performance of computer instructions, other than those required to initiate the operation.

4-8. DETAILED THEORY.

4-9. REFERENCE INFORMATION.

4-10. The following paragraphs present general information which is required for understanding the detailed theory discussion that follows.

4-11. BINARY VOLTAGE LEVELS. The binary signal levels on both interface cards are approximately +3.5 volts and +0.2 volts. The levels may vary from these approximate amounts, depending on the type of integrated circuit providing the signal. The input and output voltage levels for each type of integrated circuit are specified in section V of this manual.

4-12. LOGIC CIRCUITS. The logic circuits on both interface cards principally employ positive logic. That is to say, all inputs to an "and" or "nand" gate must be +3.5 volts for coincidence to occur. Similarly, if any input to an "or" or "nor" gate is +3.5 volts, the output is +3.5 volts for an "or" gate or +0.2 volts for a "nor" gate. The output from the "set" side of a flip-flop is approximately +3.5 volts when the flip-flop is set, and +0.2 volts when the flip-flop is reset. As an exception to the use of positive logic, diodes CR1 through CR10 on the data card, together with the circuits to which they connect on the command card, form a negative "and" gate. Also, "nand" gates MC84B, MC123A, and MC124B on the data card, and "nand" gates MC14A, MC24A, and MC44A on the command card, are used as negative-logic "nor" gates.

4-13. In accordance with established usage for positive-true logic circuits, the term "true" in this manual refers to a nominal signal level of +3.5 volts, and "false" refers to a nominal level of +0.2 volts.

4-14. ABBREVIATIONS. Signal-name abbreviations are listed in tables 5-3 and 5-5, together with the meanings of the abbreviated designations. For the meanings of abbreviations and letter symbols which are not signal names, refer to tables 4-2, 4-3, and 6-2.

4-15. SIGNAL NAMES. Signals which enter or leave the two interface cards are named in one of the following ways:

a. As a condition which either exists or does not exist.

b. As a command or order, expressed in the imperative grammatical mode.

c. In accordance with the name of a flip-flop which is the source of the signal.

d. In accordance with the name of the bus which carries the signal.

4-16. Since most of the circuits on the two interface cards employ positive logic, signal names are positive-true. The following paragraphs describe the expression "positive-true name" as applied to each of the four types of signal names.

4-17. When a signal is named in accordance with a condition, the signal level is +3.5 volts when the condition exists, and +0.2 volts when the condition does not exist. For instance, the TO (track origin) signal is +3.5 volts when the disc track origin is passing the read/write heads, and +0.2 volts when the track origin is not passing the read/write heads. Similarly, the "not" RY signal is +3.5 volts when the disc is not ready, and +0.2 volts when it is ready.

4-18. In further accordance with the principle of positive-true signal names, a signal which is named in the imperative mode becomes +3.5 volts to bring about the action commanded. For instance, the Flag FF is cleared when the CLF (clear flag) signal changes from +0.2 volts to +3.5 volts.

4-19. When a signal is named in accordance with the flip-flop which is its source, the signal taken from the set side of the flip-flop is +3.5 volts when the flip-flop is in the set condition, and +0.2 volts when the flip-flop is in the reset condition. For instance, when the Control Bit FF is set, the CB signal is +3.5 volts.

4-20. When a signal is named in accordance with the bus which carries it, the signal is +3.5 volts when the bus carries a logic 1, and +0.2 volts when it carries a logic 0.

4-21. DISC SIGNALS. All control signals and data signals that enter or leave the disc pass through the two interface cards. The control signals are illustrated in figure 4-1. The operating and service manual for the disc memory provides information on the timing of signals originating in the disc.

4-22. MULTIPLE DISCS. If more than one disc is connected to the computer, each disc has its own interface kit.

4-23. LOCATION OF CONTROLS. Table 4-1 gives the location of controls mentioned in the detailed theory discussion in this section.

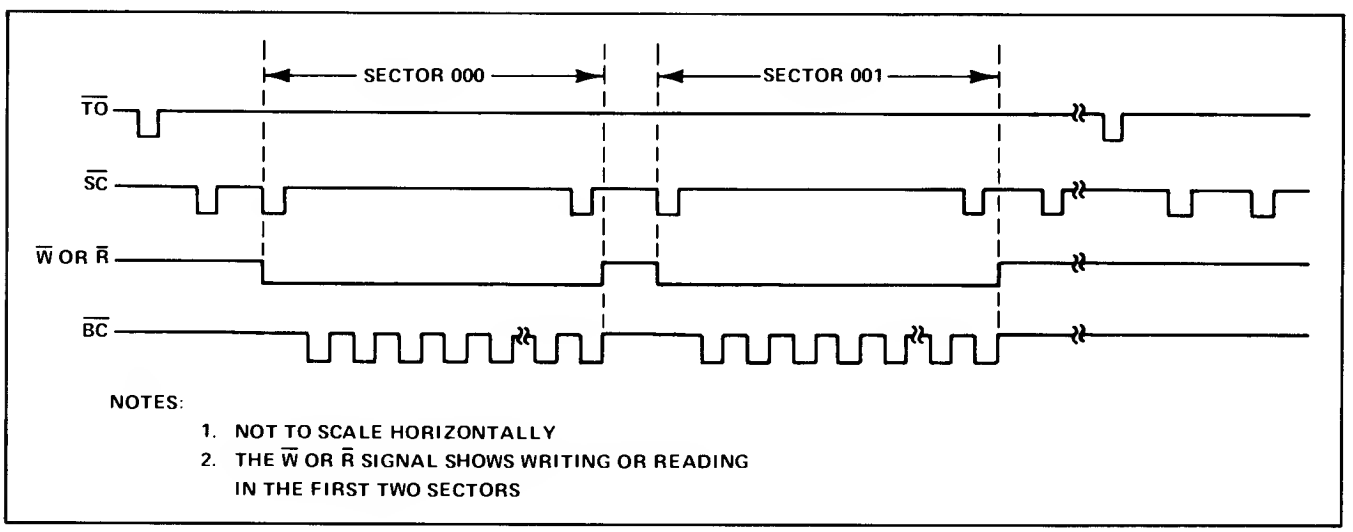
Table 4-1. Location of Controls

CONTROL	LOCATION
PRESET switch	Computer
POWER switch	Computer
Power ON switch	Disc power supply

4-24. ADDITIONAL INFORMATION. Logic diagrams for the two interface cards are furnished in figures 5-3 and 5-5, in section V of this manual. Interconnections between the two cards, and between each card and the disc memory, are listed in tables 5-3 and 5-5. In the logic diagrams and tables, pins marked with an asterisk plug into the 48-contact interface connector. Pins without an asterisk plug into the 86-contact backplane connector.

4-25. Connections from the cards to the computer are listed in the backplane wiring list for the computer.

4-26. Tables 4-2 and 4-3 list the flip-flops and registers on the two interface cards, and briefly describe the functions they perform.



2032-2

Figure 4-1. Control Signals Transferred to and from Disc Memory, Timing Chart

Table 4-2. Data Card Flip-Flops and Registers

FLIP-FLOP OR REGISTER	FUNCTION
Control Bit FF	Set by an STC instruction that uses the I/O select code of the data card. Reset by a CLC signal generated by the DMA system. Can also be reset by a CLC instruction performed by the computer, using the I/O select code of the data card. When set, initiates transfer of data to or from the disc. Remains set during and between disc sectors. When reset, terminates disc operation at the end of the current disc sector.
Data Shift Register	When writing, furnishes data to the disc in serial form. When reading, receives data from the disc in serial form. Flip-flop D0 contains the low-order bit before shifting starts (when writing) or after shifting ends (when reading).
Flag FF	Set when a new word is needed for transfer to the disc (when writing), or set when a new word has been acquired from the disc (when reading). Initiates action by DMA to furnish another word (when writing), or to acquire the new disc word (when reading). Cleared by a CLF signal received from DMA. Can also be cleared by a CLF instruction that uses the data card I/O select code.
Input Register	Used only when writing on disc. Receives from DMA each word to be written, and holds it for loading into the data shift register. Flip-flop I0 contains the low-order bit.
Output Register	Used only when reading from the disc. Receives from the data shift register each word read from the disc, and holds the word until DMA acquires it. Flip-flop O0 contains the low-order bit. Contents are changed each time a new word read from the disc is furnished by the data shift register.
Read Parity (RP) FF	Performs a meaningful function during disc reading only. Reset by the STC instruction that initiates a read operation. Toggled by each logic zero read from the disc. If set at the end of a 17-bit word, a parity error exists, and the RPE FF on the command card is set. After the first parity error of a read operation, the RP FF ceases to perform a useful function.
Track Address Register	Contains the address of the track in which writing or reading will take place or is taking place. Flip-flop TA0 contains the low-order bit. The register is loaded by bits 13 thru 7 of a word transferred from the computer by an OTA/B instruction addressed to the command card. The register retains its contents after completion of the write or read operation until another OTA/B instruction loads a new address in the register.
Write Parity (WP) FF	Used to furnish the parity bit when writing on the disc. Set before start of writing each word, then toggled by each logic 1 sent to the disc. After 16 data bits have been transferred to the disc, the WP FF is in the condition for furnishing the parity bit. Odd parity is used.

4-27. The figures and tables mentioned above should be referred to as necessary while reading the detailed theory discussion which follows.

4-28. POWER—ON INITIALIZATION.

4-29. When power is applied to the computer by the POWER switch, CRS and POPIO signals are supplied to the data card for approximately 40 milliseconds. These signals, consisting of a series of T5 pulses, are inverted on the data card, and clear the Control Bit FF and Flag FF. The inverted signal is also forwarded to the command card as "not" CRF, where it clears the Run FF. When the Run FF is in the reset condition, the "not" R and "not" W signals are true, preventing disc reading or writing that could result from the unpredictable state of flip-flops during and after power turn-on. When the computer is not running, pressing the PRESET switch also generates the CRS signal, producing the same results as at power turn-on.

4-30. To further ensure that disc writing does not take place during the transient conditions of the power turn-on period, the PON signal from the power fail interrupt card is applied to the base of transistor Q1 on the command card. The PON signal is false for about 40 milliseconds during and after power turn-on. For this period of time it keeps transistor Q1 cut-off, providing protection against disc writing. In addition, the PON signal is false during the power turn-off period, providing protection at that time also.

Table 4-3. Command Card Flip-Flops and Registers

FLIP-FLOP OR REGISTER	FUNCTION
Abort Store (ABS) FF	Cleared when an STC instruction addresses the data card. Set when the "not" RY or "not" ACL signal becomes true, or when the disc is disconnected from the command card. The state of the Abort Store FF can be determined by examining bit 3 of the disc status word. (Refer to table 3-2.)
Bit Counter	Counts "not" BC pulses received from the disc when writing or reading takes place. Flip-flop B0 contains the low-order bit. When 15 pulses have been received, the counter contains a binary 1 in each position, and an associated "nand" gate indicates the approach of the end of a word being transferred serially to or from the disc. The 16th "not" BC pulse clears the counter, and the 17th attempts to advance the counter to 1. However, the WRD FF is then in the reset condition, and the counter is held in the cleared state. The counter thus contains zero at the start of the next word. The bit counter is also cleared at the start of each sector by the second "not" SC pulse of the sector. The bit counter runs only when disc writing or reading takes place.
Direction (DI) FF	Indicates whether disc writing or reading is taking place. Set for writing, reset for reading, by an OTA/B instruction that addresses the command card.
End-Of-Sector (EOS) FF	Indicates when the end of a sector is reached on the disc. Set at the end of the 64th word in the sector, and reset by the leading edge of the second "not" SC pulse of the next sector.
Read-Parity Error (RPE) FF	Performs a meaningful function during disc reading only. Checks the state of the RP FF at the end of reading each word. If the RP FF found an odd number of logic 0's in the word (a parity error condition), the RPE FF is set. The RPE FF remains set, regardless of additional parity errors, until an STC instruction addresses the data card. The state of the RPE FF can be examined by checking bit 1 of the disc status word.
Run FF	Set at the leading edge of the second "not" SC pulse for a sector in which disc reading or writing will take place. Reset at the end of each sector.
Sector Address Coincidence FF	Indicates that the sector specified for disc reading or writing has been reached. Set by the first "not" SC pulse of the specified sector. Reset when disc operation is completed or aborted.
Sector Address Register	Receives the address of the sector in which disc writing or reading will start. Flip-flop S0 contains the low-order bit. The register is loaded by bits 6 thru 0 of a word transferred from the computer by an OTA/B instruction addressed to the command card. The register retains its contents until a new sector address is loaded.
Sector Clock Phase (SCP) FF	In the set condition between the trailing edges of each pair of "not" SC pulses. Serves as a divide-by-two counter for the sector counter input, and is also used to differentiate between the first and second "not" SC pulses.
Sector Counter	Contains a binary number that is one greater than the address of the disc sector passing the read/write heads. Flip-flop SC0 contains the low-order bit. The counter is advanced by the second "not" SC pulse of each sector, and is cleared each time track origin passes the read/write heads.
Strobe (STR) FF	Set at the start of each word read or written. Reset at the end of each word read or written. Controls the transfer of data from the data shift register to the output register (when reading), or from the input register to the data shift register (when writing) on the data card. Also controls setting of the WP FF on the data card (when writing), and the application of SRQ requests to the DMA system.

Table 4-3. Command Card Flip-Flops and Registers (Continued)

FLIP-FLOP OR REGISTER	FUNCTION
Track Origin Store (TOS) FF	Reset by a CLF instruction which addresses the command card. Set when the track origin is reached. Remains set until cleared by another CLF instruction.
Word Counter	Counts words transferred to or from the disc. Flip-flop WD0 contains the low-order bit. The counter is reset by the second "not" SC pulse of each sector. The counter runs only during transfer of data to or from the disc.
Word (WRD) FF	When transferring words to or from disc, indicates when the end of each word is reached. Set at the start of each word transferred, reset near the end of each word.

4-31. As well as clearing the Run FF, the "not" CRF signal clears the sector address register (flip-flops S6 through S0) on the command card. This is done through MC14A, which functions as a negative-logic "nor" gate.

4-32. When the power ON switch on the disc power supply is set to the ON position, the disc starts to rotate and the disc memory supplies a true "not" RY signal to the command card until the disc reaches operating speed. The "not" RY signal is inverted on the command card, and it clears the SAC FF and sets the ABS FF.

4-33. If the disc is not connected to the computer, the "not" RY input pin to the command card faces an open circuit. The open input to inverter MC65A produces the same result as if the "not" RY signal were true. Other faults which will keep the "not" RY signal true are the following:

a. The circuit in the disc memory which supplies the "not" RY signal is defective.

b. The disc memory is not connected to the disc power supply.

c. No line voltage is applied to the disc power supply.

d. The disc power supply is defective or not turned on.

4-34. When the disc is ready for use, the "not" RY signal becomes false. Through "and" gate MC67A on the command card, the inverted "not" RY signal can be gated onto the IOBI7 line. This occurs when an LIA/B instruction addresses the command card. The instruction places all IOBI bits from the command card into the A- or B-register in the computer. These bits constitute the disc status word, and bit 7 will indicate whether the disc is ready for use. (Refer to table 3-2.)

4-35. After the power turn-on period the sector counter, on the command card, assumes an unpredictable condition. (Flip-flops SC6 through SC0 make up the sector counter.) The first "not" TO pulse received from the disc resets the counter to zero, after which it functions in synchronism with the "not" SC pulses received from the disc. Figure 4-2 is a timing chart showing the operation of the counter and its associated SCP FF.

4-36. It should be noted that the SCP and SC6 through SC0 FFs are of the dual-rank JK type. The positive-going clock input to each flip-flop gates the signal input into the first rank of the flip-flop. The negative-going clock input transfers the original signal input to the output rank of the flip-flop.

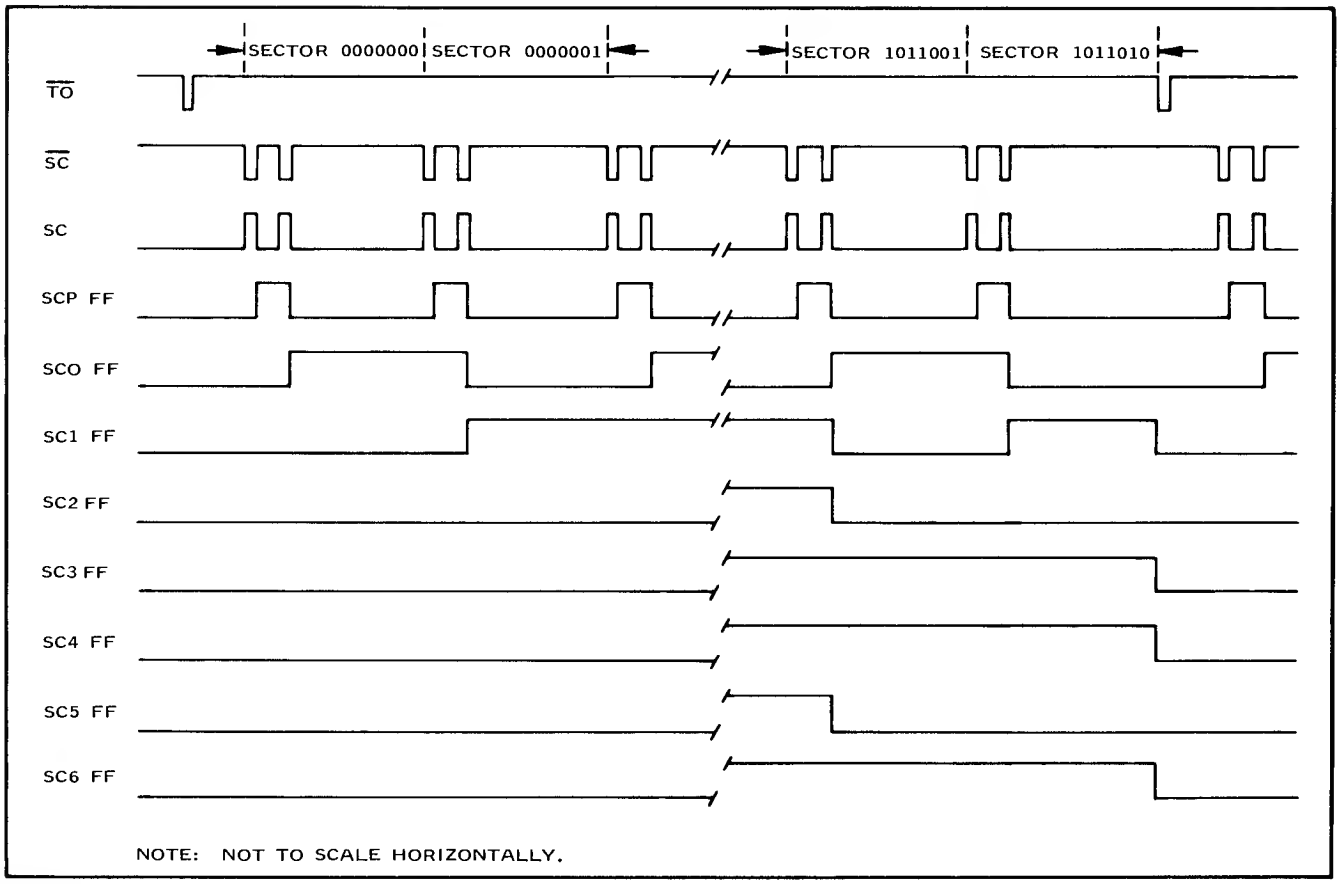
4-37. Each pair of "not" SC pulses advances the sector counter by 1, with the SCP FF functioning as a divide-by-two counter preceding the sector counter. The change of the output rank flip-flops in the sector counter takes place at the trailing edge of the second "not" SC pulse of each pair.

4-38. The first pair of "not" SC pulses after the "not" TO pulse advances the counter to 00000001, binary. This number is one greater than the address of the sector that is about to come under the read-write heads. The counter continues to function in this manner for each sector in the track. When the last sector has passed, the "not" TO pulse clears the counter.

4-39. A voltage transient or momentary equipment failure could result in incorrect contents in the sector counter and the SCP FF. If this occurs, the next "not" TO pulse will return the counter and SCP FF to their proper state, restoring normal operation. Every "not" TO pulse sets the TOS FF.

4-40. The address of the next disc sector can be gated onto the IOBI14 through 8 lines, and placed in the A- or B-register in the Computer, by an LIA/B instruction that addresses the command card. (Refer to table 3-2, bits 14 through 8.)

4-41. The set state of the SCP FF indicates that the sector counter is about to be advanced. This advance occurs when the SCP FF is reset. The condition of the SCP FF can be sampled by an LIA/B instruction which addresses the command card. When this instruction is executed, the IOBI outputs from the command card are loaded into the computer A- or B-register as the disc status word, and bit 15 of the status word can then be examined by the program to determine the state of the SCP FF. (Refer to table 3-2.) If the SCP FF is set (bit 15 of the status word is logic 1, the next sector is about to pass under the read/



2032-3

Figure 4-2. Sector Counter Timing Chart

write heads. Consequently, it is too late in the current disc revolution to start a write or read operation in the sector indicated by the sector select register (bits 14 through 8 of the status word). If an attempt is made to start such an operation, it will not begin until two disc revolutions later. During these revolutions the Run FF remains set. The set-side output of the Run FF is furnished to diode CR1, which forms one input of a 2-input "or" gate made up of CR1, CR2, and the input circuit of "and" gate MC37B. If, during the 2-revolution waiting period, an LIA/B instruction acquires the disc status word, "and" gate MC37B forwards the output of the CR1-CR2 "or" gate to IOBO line 0 as bit 0 of the disc status word. Since the Run FF is set at this time, bit 0 of the status word will be logic 1, indicating that the disc is busy. (Refer to table 3-2.)

4-42. It has been seen that after power is applied to the computer and disc, the trailing edge of the first "not" SC pulse after the first "not" TO pulse sets the SCP FF. With this flip-flop set, the second "not" SC pulse (inverted) clears the word counter and EOS FF on the command card through "nand" gates MC54E and MC64E. Also, "nand" gate MC34B sets the STR and WRD, FFs, and clears the bit counter. (Gate MC44A, used in clearing the bit counter, functions as a negative-logic "nor" gate.)

4-43. To summarize the initial condition of the data card and command card after power is applied to the computer and the disc, flip-flops and registers are in the following condition:

a. The Control Bit FF is reset.

b. The Flag FF is reset.

c. The Run FF is reset.

d. The SAC FF is reset.

e. The ABS FF is set.

f. The sector counter contains the address of the next disc sector, and is running.

g. The word counter is reset and not running.

h. The EOS FF is reset.

i. The bit counter is reset and not running.

j. The STR FF is set.

k. The WRD FF is set.

l. The RP FF is set.

m. The TOS FF is set.

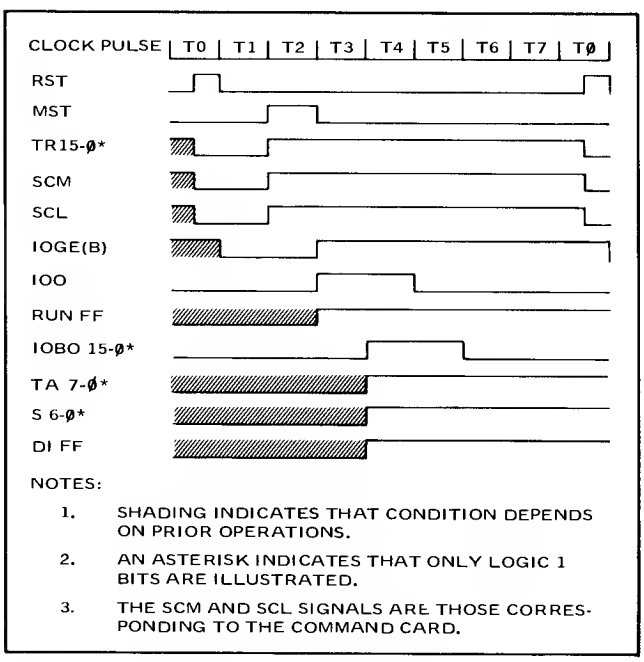
4-44. Other flip-flops and registers on the interface cards could be either set or reset.

4-45. When the command card is addressed by an LIA/B instruction, no change is made in the state of flip-flops on the interface cards. However, when disc reading or writing is initiated, flip-flops are set or cleared as required to start the operation, and the word counter and bit counter start running.

4-46. WRITE OPERATIONS.

4-47. GENERAL. Disc writing requires that the computer initialize the DMA system, then furnish a CW4 word to the disc system by means of an OTA/B instruction addressed to the command card. (The CW4 word is described in section III of this manual.) The computer then initiates writing by executing an STC instruction addressed to the data card.

4-48. OTA/B INSTRUCTION. The CW4 word specifies whether a read or write operation will be performed, and specifies the track and sector in which reading or writing will start. (Refer to table 3-3.) When the OTA/B instruction which supplies this word is executed, the T-register in the computer is reset in the last half of computer time period T0 (see figure 4-3). Then, during T2, the instruction is read from the core storage unit in the computer, and placed in the T-register. The OTA/B instruction is decoded, and the appropriate SCM and SCL signals become true. (There are eight each of the SCM and SCL signals, corresponding to the eight high-order and eight low-order octal digits of the range of I/O select codes that can be used. The signals which become true are those that specify the I/O select code of the command card.)



2032-4

Figure 4-3. OTA/B Instruction and Resulting Disc System Operations, Timing Chart

4-49. At T3 the IOGE(B) and IOO signals come true. With SCM, SCL, IOGE(B), and IOO all true, "nand" gate MC15B on the command card furnishes a false output during T4 which ensures that the Run FF is in the reset condition. Also, pin *19 of the command card furnishes a false "not" STA signal to pin *19 of the data card to ensure that the Control Bit FF is reset. The resulting false CB signal furnished to pin *W of the command card ensures, in turn, that the SAC FF is reset.

4-50. If the Control Bit FF was in the set condition, a prior disc read or write operation was in progress. Resetting the Control Bit FF will immediately terminate the former operation. The Run, and SAC FFs might also have been set, hence the necessity for ensuring that they are in the reset condition before a new operation is started.

4-51. At T4, the computer places CW4 on IOBO lines 15 through 0. The bit positions of CW4 retain their identification when CW4 is places on the lines. That is, the bit in position 15 of the A- or B-register is gated onto IOBO line 15, the bit in position 14 of the register is gated onto IOBO line 14, etc.

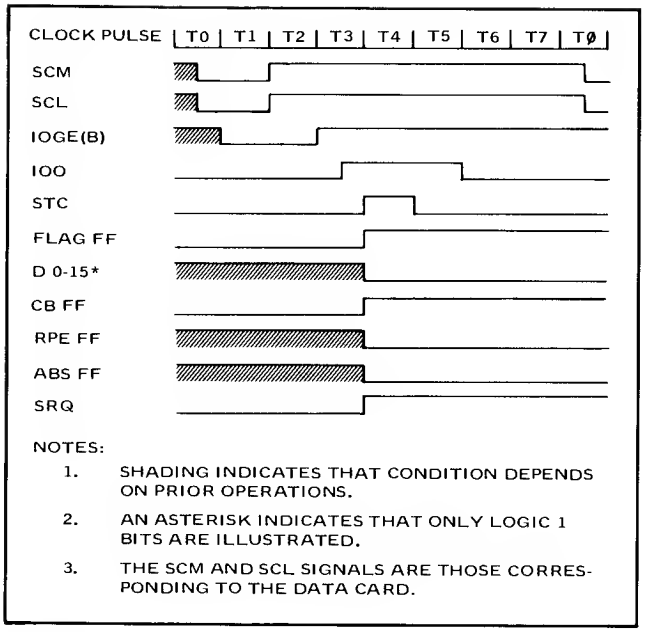
4-52. The track address, on IOBO lines 13-7, is clocked into the track address register on the data card by "nand" gate MC84B. (Presently unused, flip-flop TA7 allows for future expansion in track capacity.) On the command card, the sector address, furnished on IOBO lines 6 through 0, is clocked into the sector address register by "nand" gate MC14A. (This gate functions as a negative-logic "nor" gate.) The loading of the track and sector address registers takes place at T4.

4-53. Also at T4, the DI FF on the command card is set by the logic 1 on IOBO line 15. The logic 1 on IOBO line 15 corresponds to the 1 in bit position 15 of the CW4 word. This 1 indicates that disc writing, rather than reading, will be performed

4-54. Although the OTA/B instruction is addressed to the command card, the data on IOBO lines 13 through 7 is loaded into the track address register on the data card. This is made possible by the false STA input applied to pin *19 of the data card.

4-55. STC INSTRUCTION. When the computer decodes the STC instruction which initiates disc writing, SCM and SCL signals that address the data card become true at the start of T2. (See figure 4-4.) Signal IOGE(B) becomes true at T3, and the STC signal is true during T4. The STC signal is furnished to the data card, where it sets the Flag FF through "nand" gate MC14B. The output of this gate also resets the data shift register.

4-56. The STC signal, inverted and gated by "nand" gate MC16B, also sets the Control Bit FF and resets the RP flip-flop. To reset the RP flip-flop, the gated and inverted STC signal is applied to pin 2 of "nand" gate MC123A. This gate functions as a negative-logic "nor" gate, and when its output becomes true the false output of "nor" gate MC23B



2032-5

Figure 4-4. STC Instruction and Resulting Disc System Operations, Timing Chart

clears the RP flip-flop. The output of MC23B is false because the "not" run signal is true. (The Run FF was reset by the OTA/B instruction that preceded the STC instruction.) The gated and inverted STC signal is also forwarded to the command card, where it resets the RPE and ABS flip-flops. (The resetting of the RP and RPE flip-flops is meaningful only when a disc read operation is initiated.)

4-57. With the Flag FF in the set state, a true SRQ signal is sent to the DMA system by the data card.

4-58. Upon receipt of the SRQ signal, the DMA system acquires from the computer memory the first word to be written on the disc, and places the word on IOBO lines 15 through 0. Then the DMA system furnishes the following signals to the data card: SCM, SCL, IOGE(B), and IOO. Upon receiving these signals, "nand" gate MC84A on the data card furnishes a clock input to the I16 through I0 FF's of the input register, and the word on the IOBO lines is loaded into the register. (Flip-flop I16 receives no input from pin 73. The - 2 volts applied to resistor MC115R2 furnishes a logic 0 to the flip-flop.) DMA also generates a CLF signal, resetting the Flag FF on the data card.

4-59. No further operations take place until the correct sector is reached on the disc. During this interval the Control Bit FF on the data card remains set, and if an LIA/B instruction acquires the disc status word, bit 0 of the status word (the busy bit) will be logic 1. As noted earlier, diodes CR1 and CR2 form the input elements of an "or" gate, and if either the Control Bit FF or the Run FF is set, bit 0 of the status word is logic 1.

4-60. If a CLC instruction addresses the data card while the starting sector is being awaited, the Control Bit FF on the data card will be cleared by a CLC signal, and the disc operation will be aborted before any data is transferred. This programmed abort does not set the ABS FF.

4-61. DISC WRITING. Disc writing is described in paragraphs 4-62 through 4-107.

4-62. Sector Coincidence. Writing begins when the starting sector is reached on the disc. It has been seen that the address of this sector is placed in the sector address register by an OTA/B instruction. It has also been seen that the current next-sector address is in the sector counter. The contents of the register and counter are compared by "and" gates and MC75A and B, MC105A through D, MC95A through D, MC85A through D, on the command card. These gates compare the set-side outputs of the counter flip-flops with the reset-side outputs of the register flip-flops. They also compare the reset-side outputs with the set-side outputs of the register. When the numbers in the counter and the register are unlike, one or more of the "and" gates encounters coincidence, and furnishes a true signal to one of the "nor" gates MC105E, MC95E, MC85E, or MC75E. The outputs of the three "nor" gates are "or" tied. Thus if the numbers in the counter and the register are unlike, a false output is provided by the "nor" gates.

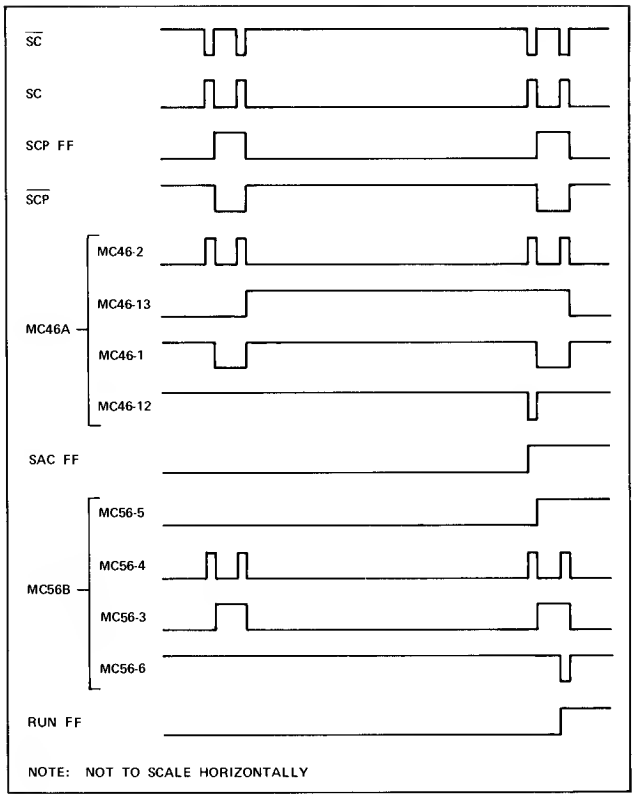
4-63. When the numbers in the counter and register are alike, none of the "and" gates encounters coincidence, all inputs to the four "nor" gates are false, and the output of these four gates becomes true.

4-64. It will be noted that "nor" gate MC75E receives inputs from "and" gates MC75D and MC75C. These two "and" gates are permanently connected to MC75E within the integrated circuit that contains all the MC75 gates. To prevent MC75D and MC75C from furnishing true signals to MC75E, the inputs to the two "and" gates are connected to ground.

4-65. It will also be noted that pin 11 inputs to MC105E, MC95E, MC85E, and MC75E are connected together, as also are the pin 12 inputs. By connecting the pins in this way, with no signal or enable input applied to them, the outputs of the three "nor" gates are caused to "or" together.

4-66. Sector Coincidence FF. When address coincidence is encountered, the output of the four "nor" gates becomes true. This true signal is applied to "nand" gate MC46A. The two other inputs to this gate are the reset-side output of the SCP FF, and the SC (inverted "not" SC) pulse. Figure 4-5 illustrates the signals applied to the gate. In the illustration, "nand" gate input and output signals are identified by the pin numbers of the gate.

4-67. As the illustration shows, coincidence for "nand" gate MC64A does not occur until one disc sector after address coincidence takes place. The circuits are designed to operate in this fashion because the number in the sector counter is one greater than the address of the sector under the read/write heads.



2032-6

Figure 4-5. Sector Coincidence, Timing Chart

4-68. The output of the SAC FF is applied to "and" gate MC57A. This gate is enabled when the computer acquires the disc status word with an LIA/B instruction. The instruction gates the IOBI lines into the A- or B-register of the computer, and by examining the state of the IOBI 5 bit, the program can determine whether the SAC FF is set.

4-69. Run FF. As figure 4-5 shows, the SAC FF is set by the first "not" SC pulse of the desired sector. The output of this flip-flop is furnished to "nand" gate MC56B, which allows the Run FF to be set by the second "not" SC pulse. MC56B also furnishes a false signal to inverter MC55D, which forwards a true RFW signal to pin *U on the data card. At this time, pins *T, *S, and *17 on the data card are also receiving true inputs. (The "not" EWW input to pins *S and *17 is true because the STR FF on the command card is set.) When the RFW input to pin *U becomes true, "nand" gate MC15B on the data card experiences coincidence, and its output becomes false. As a result, the output of "nand" gate MC124B on the data card becomes true. (MC124B functions as a negative logic "nor" gate.) The true output of MC124B causes the contents of the input register on the data card to be gated into the data shift register. This word, previously received from the DMA system, will be the first word written on the disc. Also, the WP FF is reset and the Flag FF is set.

4-70. When the Flag FF is set, it forwards a true SRQ signal to the DMA system. DMA responds by placing the next word on the IOBO lines, and by generating CLF, IOO, IOGE(B), SCM, and SCL signals. The SCM and SCL signals address the data card. The CLF signal, gated by "nand" gate MC16C, resets the Flag FF. The IOO signal, gated by "nand" gate MC16D, transfers the new word from the IOBO lines into the input register on the data card.

4-71. Returning to the Run FF, when it becomes set it furnishes a true input to "nand" gate MC46C. One of the other inputs to the gate is received from the set-side output of the DI FF. This flip-flop is in the set condition when writing takes place. The other input to MC46C is the "not" TP signal received from the data card. If track protection does not exist, "not" TP is true, and MC46C furnishes a false output. As a result, transistor Q1 conducts, and the "not" W signal changes from approximately +2.5 volts to approximately +0.3 volts. Writing on the disc then starts.

4-72. The reset output of the Run FF is furnished to "nand" gate MC37B. As noted earlier, an LIA/B instruction which acquires the disc status word enables "nand" gate MC37B. This gate furnishes bit 0 of the status word. If the Run FF or Control Bit FF (or both) is set, bit 0 of the disc status word will be 1, indicating that the disc is busy.

4-73. Write Control Operations. Figure 4-6 illustrates the signals which control disc writing and reading. Included in the illustration are bit values for typical data words. At the beginning of each sector, the word counter and bit counter are cleared by the second "not" SC pulse. When a "not" W signal from the command card initiates a disc write operation, "not" BC pulses start. The leading (negative-going) edge of each of these steps the bit counter on the command card, indicating that a bit has been written on the disc. At the leading edge of the 15th pulse all positions at the bit counter contain logic 1, and "nand" gate MC44B is enabled. (The "nand" gate output is identified in figure 4-6 by its output pin, MC44-8.) With the "nand" gate output negative, the leading edge of the next (16th) "not" BC pulse (inverted) resets the WRD FF, indicating that 16 data bits have been transferred. Also, the 16th "not" BC pulse clears the bit counter. With the WRD FF reset, the STR FF is reset by the trailing (positive-going) edge of the 16th "not" BC pulse. Then, at the leading edge of the 17th "not" BC pulse, the WRD FF is again set.

4-74. The leading edge of the 17th pulse also attempts to set FF B0 of the bit counter. However, because of the circuit delay in setting the WRD FF, and delay in MC44A and MC45E, the reset condition of the WRD FF holds B0 in the reset state. (MC44A functions as a negative-logic "not" gate.) With the WRD FF set and the STR FF reset, coincidence occurs for "nand" gate MC104A on the command card. (The output of this gate is identified in figure 4-6 as MC104-6. Also shown in the illustration is MC84-8, the corresponding gate-output for read operations.) The false output of MC104A is forwarded to pins *S and *17 on the data card as the "not" EWW signal. At this time, the input to pin *T on the data card is true because the DI flip-flop is set, and the input to pin *U on the data card is false because "nand" gate MC56B on the command card is not enabled due to the reset condition of the SCP FF. (Refer to figure 4-2.) On the data card, "nand"

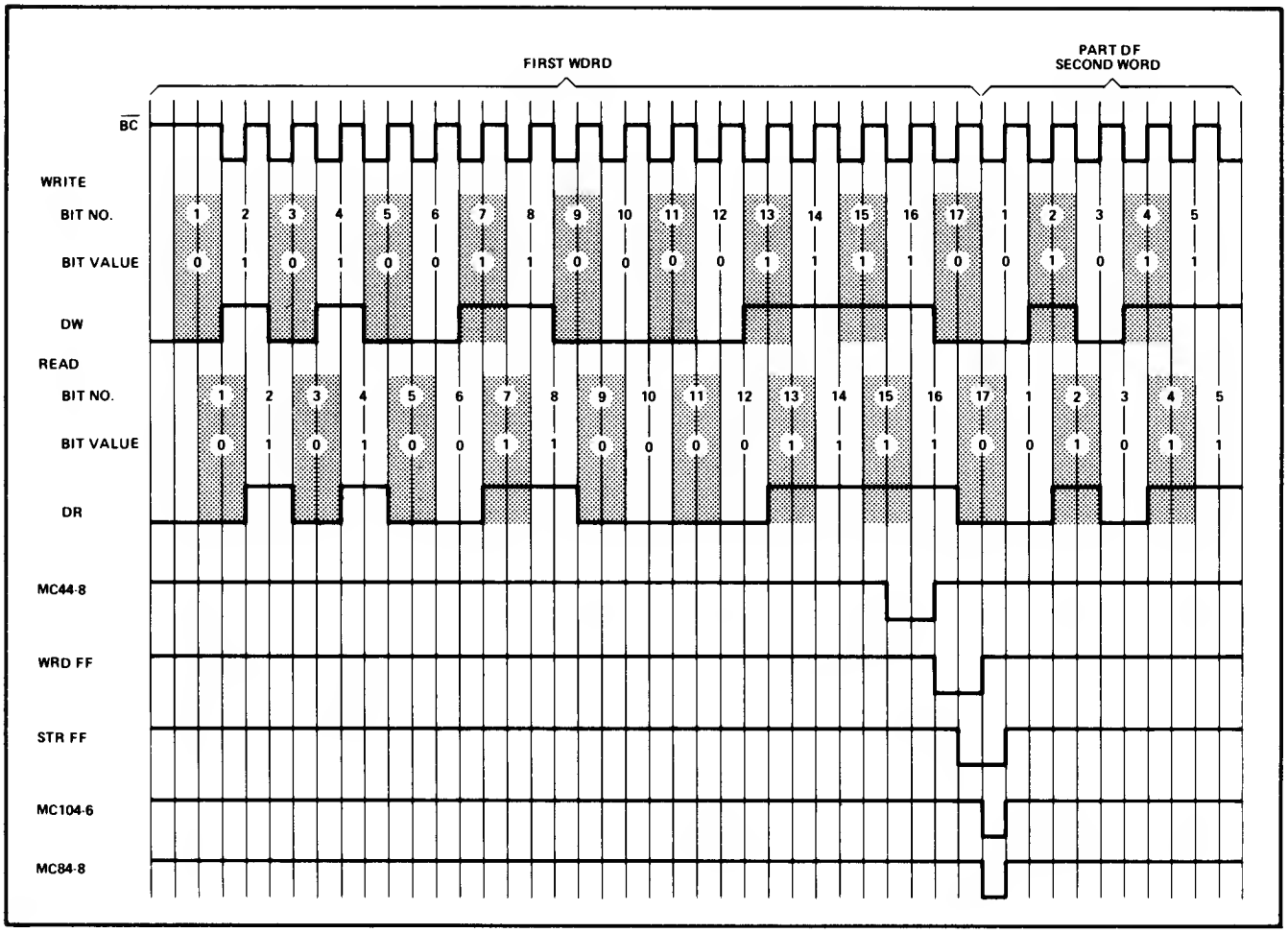


Figure 4-6. Write and Read Control, Timing Chart

gate MC15B is disabled by the false input to pin *U of the card. The input to pin 12 of "nand" gate MC124B on the data card therefore is true.

4-75. Returning to "nand" gate MC104A on the command card, its output, furnished to pins *S and *17 of the data card, is true until the WRD FF is set at the end of a word. Then, while the STR FF remains in the reset condition, the input to pins *S and *17 of the data card is false.

4-76. Coincidence no longer exists for "nand" gate MC124B on the data card, and its output becomes true. This true output gates the contents of the input register into the data shift register. At the same time, the WP FF on the data card is reset and the Flag FF is set. The Flag FF sends an SRQ signal to the DMA system indicating that the second word is required for the input register on the data card. When the word is supplied, SCM, SCL, IOGE(B), and IOO signals from the DMA system gate the word into the input register on the data card, and a CLF signal from DMA resets the Flag FF.

4-77. Note that prior to the first word stored in each sector the actions described in the preceding paragraph are brought about by a true input to pin *U on the data card. For subsequent words in the sector, the same actions are brought about by a false input to pins *S and *17.

4-78. When the WRD FF is set near the end of the first word, the positive-going edge of the 17th "not" BC pulse sets the STR FF. At this time, the word counter is advanced by binary 1, to indicate that the first word of the sector has been recorded on the disc.

4-79. The procedures described for the second word are repeated for each subsequent word in the sector. After the 64th word of the sector has been written, FF WD5 on the command card is cleared, setting the EOS FF. Inverter MC34A on the command card then prevents the enabling of "nand" gate MC104A, and thereby prevents the Flag FF from requesting a word from the DMA system.

4-80. When the WRD FF is set at the end of the 64th word, "nand" gate MC56C is enabled, and the Run FF is reset. With the Run FF cleared, the "not" W output furnished to the disc becomes true, and writing ceases. (See "not" W signal in figure 4-1.)

4-81. Operations now await the second "not" SC pulse of the new sector. This pulse strobes "nand" gates MC54E

and MC64E on the command card, resetting the EOS flip-flop and ensuring that the WD5-0 flip-flops are also in the reset condition. "Nand" gate MC34B ensures that the STR and WRD FFs are in the set condition, and that the bit counter is in the reset condition.

4-82. If writing is to be continued in the next sector, the SAC FF remains set between the two sectors. As a result, when the second "not" SC pulse of the new sector occurs, "nand" gate MC56B sets the Run FF. Operations then proceed as with the previous sector, and are continued until the operation is completed in the normal manner or aborted. Termination proceedings are described later in this section.

4-83. Data Transfer to Disc. When writing takes place, each 16-bit word in the data shift register is transferred in serial form to the disc, low-order bit first. After the 16 data bits have been transferred, a parity bit is furnished as the 17th bit. The track in which writing takes place is specified by the TA7-0 bits from the data card; these bits select the appropriate read/write head.

4-84. As stated earlier, when the writing of each word takes place the disc furnishes to the command card 17 "not" BC pulses, each indicating that a bit has been written on disc and a new bit is required. After 17 pulses have been furnished, an additional 17 are furnished for the second word, and so on. The pulses are provides in a continuous train without pauses between words. However, the pulses are not furnished between sectors. Thus 1088 pulses are generated for every sector written (17 pulses for each of 64 words).

4-85. At the start of every disc sector while writing, before the first "not" BC pulse, the DW output from the data card is sampled by the disc. This output is taken from the reset side of FF D0. Since the WRD FF is in the set condition during the writing of the 16 data bits, "nand" gate MC26A on the data card is disabled, its output is true, and "nand" gate MC26C is enabled, allowing the reset output of FF D0 to be inverted and forwarded to the disc.

4-86. After sampling the bit on the DW line, the disc writes the bit in the first bit position of the sector, then starts furnishing the "not" BC pulses to the data card. The negative-going edge of each pulse is inverted, and shifts the word in the data shift register one position toward the low-order end of the register. Thus, after each shift a new bit is supplied to the DW line. This bit is written on the disc, and another register shift takes place. The process continues until all 16 data bits have been transferred to the disc. Figure 4-6 shows the timing relationships.

4-87. As each data bit is shifted out of the D0 FF, the output rank of the WP FF is toggled if the bit is a binary 1. At the start of each word the WP FF is in the reset condition. After 16 data bits have been transferred to the disc, the WP FF will be in the reset state if there was an even number of 1's in the 16-bit word, or in the set state if there was an odd number of 1's. Consequently, the output of this flip-flop will be in the required state for furnishing the parity bit. (Odd parity is used.)

4-88. On the command card, the WRD FF is reset by the negative-going edge of the 16th "not" BC pulse. As a result, "nand" gate MC26A on the data card is enabled, and the parity bit in the WP FF is forwarded to "and" gate MC26C. At this time, the D0 FF contains a binary 0, and its reset output serves as an enable for MC26A. (The binary 0 in D0 was shifted down the register from FF D16, which was reset before shifting started.) MC26C inverts the parity bit to the required form, and forwards the bit to the disc.

4-89. While the parity bit is being sent to the disc, a new word is gated into the data shift register from the input register. Then, when the negative-going edge of the 17th "not" BC pulse indicates that the parity bit has been written, the WRD FF is set. As a result, "and" gate MC26C on the data card is again ready to forward data from FF D0 to the disc. The write operation continues without interruption, with the first bit of the new word being recorded on the disc immediately after the parity bit of the preceding word.

4-90. Words continue to be transferred to the disc until the end of the first sector is reached. If additional sectors are to be written, the procedure described is repeated for each sector. The Run FF is set and reset, respectively, at the beginning and end of each sector. However, the SAC FF remains set until the operation is completed or aborted.

4-91. Incomplete Sector. If the number of words to be written is not a multiple of 64, the last sector will not be completely filled. When an operation of this type takes place, the DMA system supplies the data card with a CLC signal after it has furnished the last word. This signal resets the Control Bit FF, which in turn resets the SAC FF. However, the Run FF remains set until the end of the sector. As a result, the "not" W signal remains false and writing continues. However, the data card no longer receives SCM, SCL, IOGE(B), or IOO signals from DMA. Therefore, the contents of the input register remain unchanged. These contents will be the last word written on the disc. Each word-time for the remainder of the last sector, the contents of the input register will be gated into the data shift register and transferred to the disc as the word to be written. Thus, the last word will be repeated on the disc until the end of the sector is reached. The Run FF is then reset, the "not" W signal becomes true, and the operation ceases. Until the Run FF is reset at the end of the sector, bit 0 of the disc status word is logic 1. (As noted earlier, if either the Control Bit FF or the Run FF is set, bit 0 of the status word is logic 1.)

4-92. Track Protection. When track protect switch S1 on the data card is closed (in the down position), no tracks are protected against writing. In this nonprotect situation the "not" TP signal is true, and "nand" gate MC46C on the command card is enabled. If the track protect switch is open, the "not" TP signal is false if the track address register contains an address for a protected track.

4-93. To clarify the functioning of the track protect circuits, assume first that all tracks are protected. To bring this about, diodes CR1 through CR8 are all removed from the data card. (Refer to table 2-1.) Now, when the track protect switch is open, the "not" TP input pin on the command card (pin *16) faces an open input. Since resistor MC47R2 is connected to - 2 volts, "nand" gate MC46C on the command card is disabled. Consequently no writing can take place. If the track protect switch is then closed, the gate is enabled, writing can take place on any track, and no track protection exists.

4-94. Assume, now, that diodes CR1 through CR8 are all in place on the data card. As shown in table 2-1, track 000 (octal) is then protected when switch S1 is open. The eight diodes, together with resistor MC47R2 on the command card, constitute a negative-logic "and" gate. Diode CR9 constitutes a 9th input to the gate when S1 is closed. If all inputs to the gate are false, the output of the gate is false. With S1 open, the "not" TP signal is false only when all flip-flops in the track address register are clear. Since the register contains the track address, track 000 (octal) is protected. However, if one or more of the flip-flops is in the set condition, "and" gate coincidence does not exist, the "not" TP signal is true, and writing can be conducted. This condition exists when the track address is other than 000.

4-95. To further illustrate the functioning of the track protect circuits, assume that diode CR1 has been removed. The "and" gate now has seven inputs (not counting CR9), and the low-order flip-flop of the track address register is not examined when determining track protect status. Track protection exists when the TA7 through TA1 FFs are all in the clear state; TA0 can be either reset or set. This condition occurs when the track address is 000 or 001 (octal).

4-96. As additional diodes are removed, additional tracks are brought into protect status when S1 is open. The track addresses corresponding to the diodes removed are not examined when the circuits determine protect status. These tracks are simply given protect status at all times, provided switch S1 is open.

4-97. Abort Store FF. The STC instruction which initiates a write operation resets the ABS FF on the command card. Then, if certain fault conditions exist during all or part of the write operation, the "not" RY signal from the disc becomes true and the flip-flop is placed in the set condition. The ABS FF is also set if the "not" ACL signal from the disc becomes false; this occurs when low line voltage is applied to the disc memory power supply. After the completion of writing, the state of the ABS FF can be checked by an LIA/B instruction. If the flip-flop is set, bit 3 of the disc status word will be logic 1, indicating that the write operation possibly was not performed successfully.

4-98. The conditions which result in setting the ABS FF are the following:

a. Low disc speed.

b. The disc circuits which supply the "not" RY signal are defective.

c. Disc memory not connected to the computer.

d. Disc memory not connected to the disc memory power supply.

e. Low line voltage or no line voltage applied to the disc memory power supply.

f. Disc memory power supply defective or not turned on.

4-99. TERMINATION OF WRITING.

4-100. General. Disc writing can be terminated in two ways: by permitting all words to be transferred to the disc, or by an abort of the write operation before its completion. In the first method, the operation is terminated by the DMA system without intervention by the computer program. In the second method the operation is terminated by a programmed abort or by an automatic abort brought about by equipment failure.

4-101. Termination by DMA System. When the DMA system terminates disc writing, it issues a CLC signal to the data card after forwarding the last word to the input register on the card. The signal resets the Control Bit FF. The SAC FF on the command card is cleared by the false CB signal produced when the Control Bit FF is reset. The Run FF is reset at the end of the current sector, when the EOS FF on the command card is set. If the number of words supplied by the DMA system is not sufficient to fill the last sector, the last word furnished is repeated in each word location in the track until the end of the sector is reached. After being reset, the Run FF is not set again at the start of the new sector, as is done when writing continues. Therefore, the "not" W signal remains true and the bit on the DW line is not written on the drum at the start of the next sector.

4-102. When the "not" W signal becomes true, the "not" BC signal is no longer furnished by the disc, and the bit counter and word counter cease running. These counters are cleared at the end of the last sector written, and remain cleared until another disc write or read operation is initiated. Also, after the end of the last sector written, the WRD and STR FFs remain in the set condition. Because STR remains set, "nand" gate MC104A on the command card does not experience coincidence, and "nand" gate MC124B on the data card experiences continued coincidence. Consequently, the Flag FF on the data card remains reset and SRQ signals are no longer sent to the DMA system.

4-103. Termination by Abort. It has been noted that a write operation can be aborted in two ways: either by a programmed instruction or by the occurrence of certain faults in the disc memory or disc memory power supply.

4-104. When a programmed abort occurs, the computer performs a CLC instruction with the I/O select code of the data card. The computer furnishes a true CLC signal to pin 21 of the data card, producing the same results as the CLC signal supplied by the DMA system for normal termination.

4-105. The equipment fault termination is brought about by the "not" RY signal becoming positive during the disc write operation. This resets the SAC FF on the command card and sets the ABS flip-flop. At the end of the sector, the Run FF is reset in the normal manner, but because the SAC FF is reset, the Run FF is not set again at the start of the next sector. As a result, the "not" W signal remains true, and at the start of the next sector the bit on the DW line is not written on the disc and the "not" BC signal is not supplied. Without "not" BC pulses, the bit counter and word counter remain in the clear condition and the WRD and STR FFs remain in the set condition. Because the STR FF remains set, the Flag FF on the data card remains reset and SRQ signals are no longer sent to the DMA system. Note that if the "not" ACL signal becomes false, only the ABS FF is set. However, if the "not" RY signal becomes true, the SAC is cleared as well, terminating the operation.

4-106. If a write operation is aborted because the "not" RY signal becomes true, the DMA channel concerned becomes locked up. The word count maintained by the DMA system indicates that additional words must be supplied to the disc, but because DMA no longer receives true SRQ signals from the disc data card, it does not furnish the required words. A programmed check of the DMA channel, using an SFS or SFC instruction with the DMA channel I/O select code, will indicate that the DMA channel is busy. Furthermore, a check of the disc busy bit (bit 0 of the disc status word) will indicate that the disc is busy. The situation continues until the Flag FF on the DMA control card, and the Control Bit FF on the disc data channel interface card, are reset. These two flip-flops can be cleared by performing one of the following:

a. Start a new disc read or write operation on the DMA channel concerned, using the normal disc initiation instructions.

b. Clear the DMA Flag FF by performing a CLF instruction with the DMA channel I/O select code. Also, clear the disc Control Bit FF by performing a CLC instruction with the disc data card I/O select code.

c. Reset the entire I/O system by generating a CRS signal in any of the following ways:

(1) With the computer stopped, press the PRESET switch.

(2) Turn off computer power by means of the POWER switch, then restore power.

(3) Program a CLC instruction, using zero as the I/O select code.

4-107. Existence of DMA lockup resulting from a fault in the disc memory or disc memory power supply is indicated by bit 3 of the disc status word. If this bit is 1 after sufficient time has been allowed for completion of the data transfer, the "not" RY signal was true during the transfer, the data transfer was probably not completed and the DMA channel and disc must be cleared by one of the methods listed in the preceding paragraph. Another method of checking for the existence of the lockup condition is to perform an LIA/B instruction using the DMA channel I/O select code. This instruction places in positions 13-0 of the computer A- or B-register the number in the DMA word count register. (This register is on the DMA register card.) Bit 0 in the computer A- or B-register will contain the low-order bit of the word count. If sufficient time has been allowed for completion of the transfer, the word count should be zero.

4-108. POST—WRITE STATE. After termination of writing, either by DMA or by a programmed CLC instruction, flip-flops and registers on the disc interface cards will be in the condition listed below. The state of flip-flops and registers not listed depends on prior operations. (If an operation is terminated before the end of a sector, the bit counter and word counter remain running and the Run FF remains set until the end of the sector is reached. The RP FF is reset then set, at the end of each remaining word in the sector.)

a. The Control Bit FF is reset.

b. The Flag FF is reset.

c. The Run FF is reset.

d. The SAC FF is reset.

e. The sector counter contains the address of the next disc sector, and is running.

f. The word counter is reset and not running.

g. The EOS FF is reset.

h. The bit counter is reset and not running.

i. The STR FF is set.

j. The WRD FF is set.

k. The DI FF is set.

4-109. READ OPERATIONS.

4-110. Disc read operations are very similar to disc write operations. Therefore, only the principal functions of reading are presented, together with detailed discussion of the operations unique to the read process.

4-111. When reading is to be performed, the DMA system and disc memory are initialized in the same manner as the writing. First, an OTA/B instruction with the

command card I/O select code forwards a CW4 word to the command card and data card. This word indicates that reading will take place, and designates the starting track and sector. The track address register and sector address register are loaded in the same manner as for writing. However, bit 15 of CW4 is logic 0 when reading is to be performed, resulting in the DI flip-flop being placed in the reset condition. A further difference from the write operation is that "nand" gate MC65B on the command card furnishes a "not" HC signal to the disc during T4 of the OTA/B instruction. As a result, the "not" RI signal, supplied by the disc to the command card, becomes false at the start of T4.

4-112. After the OTA/B instruction, an STC instruction starts the disc read operation.

4-113. Sector coincidence occurs in the same manner as for writing. However, the RI signal from the disc ensures that at least a full sector elapses between the occurrence of sector coincidence and the setting of the SAC FF. Referring to figure 4-5, the MC46-13 input to the MC46A "nand" gate is shown as becoming true at the trailing edge of the second "not" SC pulse. This will occur if coincidence did not exist when the sector address register was loaded. However, if coincidence does exist when the register is loaded, MC46A will furnish a false output as soon as the next "not" SC pulse occurs. This could happen almost immediately if the sector address register is loaded near the end of a sector. The situation is not a problem with writing, but it creates a difficulty when reading because the read amplifiers in the disc memory require settling time after the sector address register is loaded. During this settling time the RI signal furnishes a false input to inverter MC65C on the command card. The resulting true input to pin 10 of "nand" gate MC65D keeps pin 8 of MC65D false. Then, if an attempt is made to set the SAC FF by the first "not" SC pulse after coincidence, the SAC FF furnishes true outputs from both the set and reset sides. Then, when the output of "nand" gate MC46A again becomes true, the SAC FF remains reset. Consequently, at the second "not" SC pulse after address coincidence, the Run FF cannot be set. After this point, sector coincidence will be effective in setting the SAC FF.

4-114. When the run flip-flop is set, the command card sends a false "not" R signal to the disc, rather than a "not" W signal as is done for writing. This difference is brought about by the reset condition of the DI flip-flop.

4-115. Upon receipt of the false "not" R signal, the disc commences to read data from the track indicated by the TA7-0 outputs from the data card. Also, "not" BC pulses are furnished to the data card (refer to figure 4-6).

4-116. The data read from the disc is furnished to the data card as the DR signal. In each word the data is received low-order bit first, and the parity bit is received last.

4-117. As it arrives from the disc, each bit is placed in the input rank of the D16 FF. This is brought about by the negative-going edge of the pulse applied to pin 3 of the D16 FF. The bit thus is acquired from the disc at the trailing (positive-going) edge of a "not" BC pulse. At the leading edge of the next "not" BC pulse, the bit is transferred to the output rank of the D16 FF. Then, the trailing edge of the "not" BC pulse transfers the bit to the input rank of the D15 FF, while at the same time a new bit is clocked into the input rank of the D16 FF. This process continues for each bit of the word.

4-118. When the bit counter indicates that 16 bits have been received, the WRD FF is reset, then set again at the start of the 17th bit. When the 17th (parity) bit has been placed in the D16 FF on the data card, the STR FF is reset, and "nand" gate MC84C on the command card experiences coincidence. The output of this gate is forwarded to the data card as the "not" EWR signal, where it sets the Flag FF and gates the contents of FFs D15-0 into the output register.

4-119. Setting the Flag FF sends a true SRQ signal to the DMA system, indicating that a word is waiting in the output register. When it is ready to acquire the word, the DMA system furnishes IOI, IOGE(B), SCM, and SCL signals to the data card. These gate the contents of the output register onto the IOBI 15-0 lines, and the word is acquired by the DMA system.

4-120. Subsequent words read from the disc are treated in the same manner as the first word. Between each sector the Run FF is clear, the "not" R signal is true, and "not" BC pulses are no longer furnished by the disc. Then, at the start of each new sector, the Run FF is set, the "not" R signal becomes false, and "not" BC pulses are furnished. In each sector 1088 bits are written (64 17-bit words), and the drum furnishes 1088 "not" BC pulses.

4-121. As each 17-bit word is received from the disc, its parity is checked by the RP FF on the data card. This flip-flop is placed in the reset state at the start of the read operation by the first "not" BC pulse received. If the RP FF is set when the leading edge of the first inverted "not" BC pulse is applied to its clock input (pin 11), the output from its own pin 9, inverted by "nor" gate MC23B, resets it. If the RP FF is already reset when the leading edge of the first "not" BC pulse occurs, no change in the flip-flop takes place.

4-122. As the bits in each word are received, they are furnished (as the DR signal) to "and" gate MC35B on the data card. This gate, in turn, forwards the data bits to "nand" gates MC34C and MC34D. As each data bit is furnished to the RP FF, there is no change in the flip-flop if the bit is a binary 1. "Nand" gate MC34C is disabled by the false input from pin 9 of the RP FF, and "nand" gate MC34D merely furnishes a clear signal to the reset flip-flop. Furthermore, the input to pin 12 of the RP FF is true, and the leading edge of each clock pulse attempts to set the RP FF. However, the false input to pin 13 of the RP FF (when a binary 1 is received) holds the RP FF in the reset state.

4-123. When a binary 0 is received, "nand" gates MC34C and MC34D are both disabled, and the clock pulse applied to the RP FF, together with the true input at pin 12 of the flip-flop, sets the RP FF. Subsequently, logic 1's will again have no affect on the RP FF; MC34C merely retains the set condition of the flip-flop, and MC34D is disabled. However, when another binary 0 is received, MC34C and MC34D are both disabled, and the clock pulse toggles the RP FF.

4-124. Operations continue in this fashion, with each logic 0 toggling the flip-flop, until the 17 bits of the word have been received. Because odd parity is used, there should be an even number of logic 0's in the word, and the RP FF should be in the reset state at the end of the word. However, if an odd number of 0's was received, a parity error occurred, and the RP FF will be set at the end of the word. When the STR FF on the command card is placed in the set condition at the end of the word, the RPE FF is placed in the same condition as the RP FF. Thereafter, the RPE FF remains set and the RP FF plays no further part in the operation. If another parity error occurs, the RP FF will be in the clear state at the end of a word. However, the RPE FF is not reset because it is held in the set condition by the false input furnished to its pin 10 by its own pin 8.

4-125. When the read operation is completed, an LIA/B instruction can acquire the disc status word, and bit 0 of the word can be examined to determine whether a parity error occurred.

4-126. The RPE FF is reset the next time an STC instruction initiates a disc operation. When this occurs, a false input is applied to pin 13 of the RPE FF, making the output from pin 8 true. With pin 8 true, the input to pin 10 is no longer effective in holding the flip-flop set.

4-127. The disc read operation can be terminated either by reading all words scheduled, or the operation can be aborted. Termination procedures are the same as for disc writing. After termination, flip-flops and registers on the disc interface cards will be in the same condition as when writing is terminated, except that the DI FF is in the reset state.

4-128. As in disc writing, a true condition of the "not" RY signal or a false condition of the "not" ACL signal sets the ABS FF. After completion of the read operation, an LIA/B instruction allows examination of the state of the flip-flop.

4-129. LIA/B INSTRUCTION.

4-130. Functions of the LIA/B instruction have been dealt with in appropriate places when discussing disc writing and reading. Operation of the instruction as a whole, as it pertains to the disc interface cards, will now be presented.

4-131. When an LIA/B instruction using the command card I/O select code is decoded, the appropriate SCM and SCL signals become true at T2. (See figure 4-7.) Then, when IOGE(B) and IOI become true, "and" gate MC27A on the command card experiences coincidence. The output of this gate is furnished to other "and" gates which forward the various bits of the disc status word to the IOBI lines. At T5TS, these bits are placed in the computer A- or B-register.

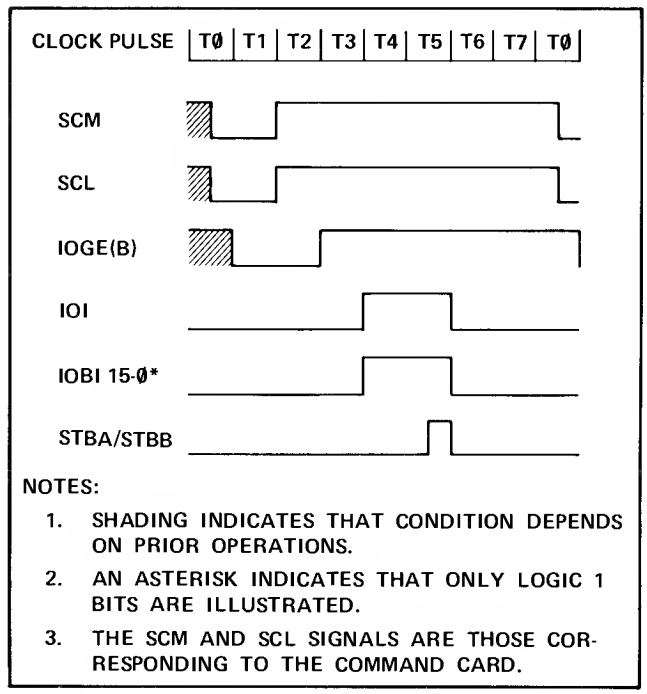
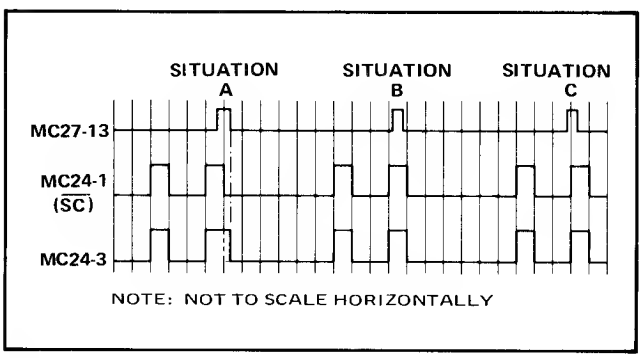


Figure 4-7. LIA/B Instruction and Resulting Disc System Operations, Timing Chart

4-132. Table 3-2 describes the significance of the various parts of the status word.

4-133. The "not" SC pulses which advance the sector counter are asynchronous with respect to computer timing. During T4 and T5, while the sector counter is being sampled by an LIA/B instruction, a "not" SC pulse could result in an arithmetic carry rippling down the counter. This would cause an erroneous indication of the next-sector address in the status word if corrective measures were not taken. "Nand" gate MC24B on the command card prevents difficulty from this source. When an LIA/B instruction is not being performed, pin 5 of the gate receives a false input, and the input to pin 2 of "nand" gate MC24A is true. MC24A then functions simply as an inverter, and allows normal advance of the sector counter. However, during T4 and T5 of an LIA/B instruction, pin 5 of MC24B is true. If no SC pulse is received during this T4-T5 time period, the input to pin 1 of MC24A is true, the output of MC24A is false, and MC24B is disabled by its pin 4. Since the sector counter is not being advanced at this time, no change in operation is needed or provided. Assume,

however, that the T4-T5 time period of an LIA/B instruction starts during the second "not" SC pulse of a sector. (See situation "A", figure 4-8.) The output from MC27-13 is true during the T4-T5 time period of an LIA/B instruction. Before the second "not" SC pulse, both inputs to MC24A are true, and the output of MC24A is false. This output disables MC24B. At the leading edge of the "not" SC pulse, MC24A no longer experiences coincidence, and its output becomes true. (MC24A functions as a negative-logic "nor" gate.) Because the sector counter is advanced by the trailing edge of the "not" SC pulse, it does not change at this time. However, pin 4 of MC24B receives a true input. Next, the T4 time period of the LIA/B instruction starts, and pin 5 of MC24B receives a true input. Since pin 4 of this gate is receiving a true input, the gate furnishes a false input to pin 2 of MC24A. When the end of the "not" SC pulse occurs, the output of MC24A remains true because pin 2 of MC24A is receiving a false input. At the end of T5, after the contents of the sector counter have been sampled, the input to pin 5 of MC24B becomes false, the output of MC24B becomes true, the input to pin 2 of MC24A also becomes true, and MC24A furnishes a false output. At this time, the sector counter is advanced. The effect has been to stretch the "not" SC pulse until the end of the T5 time period, and in so doing, prevent the advance of the sector counter until after it has been sampled.



2032-9

Figure 4-8. Delay in Sector Counter Advance, Timing Chart

4-134. Assume next that the T4-T5 time period of an LIA/B instruction occurs entirely during the second "not" SC pulse (situation "B", figure 4-8). As in situation A, the leading edge of the "not" SC precedes the leading edge of T4, and no change takes place when T4 starts. Then, when T5 ends, the input to pin 5 of MC24B becomes false, and only the false input to pin 1 of MC24A maintains a true output from MC24A. Thus, when the end of the "not" SC pulse arrives, the sector counter is advanced in the normal manner. Because the counter has already been sampled, the carry ripple (if any) produces no adverse affect.

4-135. Finally, assume that the second "not" SC pulse of a sector begins during the T4-T5 period of an LIA/B instruction that addresses the disc (situation "C", figure 4-8). Before the T4 time period starts, the output of MC24A is false. At the leading edge of T4, the input to pin 5 of MC24B becomes true. However, pin 4 of this gate receives a false input, and no change occurs in the output of the gate. When the leading edge of the "not" SC pulse occurs, MC24A provides a true output. This output furnishes coincidence for MC24B, which in turn provides a false input to pin 2 of MC24A. No change occurs in MC24A because it is receiving another false input at pin 1. At the end of T5, the input to pin 5 of MC24B becomes false, but the output of MC24A remains unchanged. Then, at the end of the "not" SC pulse, the output of MC24A becomes false in the normal manner, and the sector counter is advanced.

4-136. To summarize the control of the advance of the sector counter, its advance is delayed only when the T4-T5 time period overlaps the trailing edge of the "not" SC pulse. (It is during this time that the sector counter is being sampled.) The delay in advancing the counter is brought about by stretching the "not" SC pulse until the end of the T5 pulse. Other actions controlled by the output of MC24A are not adversely affected. The delay in the trailing edge of the "not" SC pulse occurs for both the first and second "not" SC pulses. The delay performs a meaningful function only in the case of the second "not" SC pulse, because the sector counter is advanced at the trailing edge of this pulse.

4-137. CLF AND SFS INSTRUCTIONS.

4-138. The CLF and SFS instructions are used to determine whether "not" TO pulses are received from the disc. First, a CLF instruction with the command card I/O select code is performed. This instruction resets the TO FF on the command card. Then, an SFS instruction is performed, again addressing the command card. If the TO signal was received by the command card since performance of the CLF instruction, the TOS FF is set, and a true SKF signal is forwarded to the computer by the command card. As a result, a program skip occurs. If the TO signal was not received since the CLF instruction, the SKF signal remains false, and no skip takes place.

4-139. SFC INSTRUCTION.

4-140. The SFC instruction, when addressed to the command card, causes a program skip if the SCP FF on the command card is clear. (See figure 4-2 for timing of the SCP FF.) When the SFC instruction is performed, "nand" gate MC17B on the command card senses the state of the SCP FF, and generates a true SKF signal if the flip-flop is clear.

SECTION V
MAINTENANCE

5-1. INTRODUCTION.

5-2. This section contains maintenance information for the 12606B Disc Memory Interface Kit. Included are preventive maintenance instructions, corrective maintenance instructions, and maintenance data consisting of a table of interface card connections, information pertaining to integrated circuit characteristics and connections, reference designation indexes, part location views, and schematic diagrams.

5-3. PREVENTIVE MAINTENANCE.

5-4. Preventive maintenance for the disc memory interface kit is conducted by running the entire disc diagnostic program once each month. At least three passes through the read/write portion of the program must be made, using the worst-case test word: 1100110011001100CC.

5-5. As well as testing the disc memory interface, the diagnostic program also checks the operation of the disc memory and the disc memory power supply. Instructions for running the diagnostic program are contained in the manual supplement attached to the back of this manual.

5-6. CORRECTIVE MAINTENANCE.

5-7. GENERAL.

5-8. When performing troubleshooting, refer to figures 5-1 through 5-5 and tables 5-1 through 5-5 in this section, and to figures 4-1 through 4-8.

5-9. INTERCONNECTIONS.

5-10. For connections to the 86-pin connector on each interface card, refer to the computer backplane wiring list. For connections to the 48-pin connector on each card, refer to table 5-3 or 5-5.

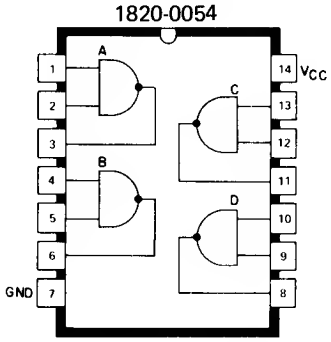
5-11. SIGNAL VOLTAGES.

5-12. The voltage levels of signals received from the disc are as follows: logic 1 is +5.1 to +2.4V (+3.5V nominal), logic 0 is +0.4 to +0.0V (+0.2V nominal).

5-13. For voltage levels of signals received from the computer, refer to computer documentation.

5-14. To determine the input voltages, output voltages, and circuit delay of integrated circuits on the disc interface cards, first locate the integrated circuit in figure 5-1 then refer to the appropriate characteristics in table 5-1. The nominal levels for all integrated circuit inputs and outputs are +3.5V and +0.2V.

1820-0054



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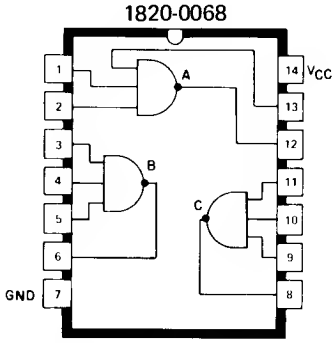

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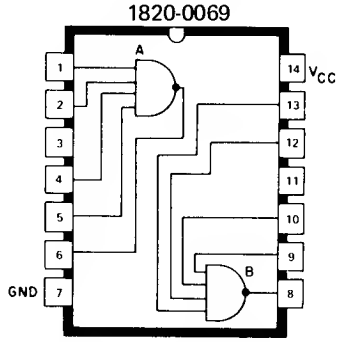

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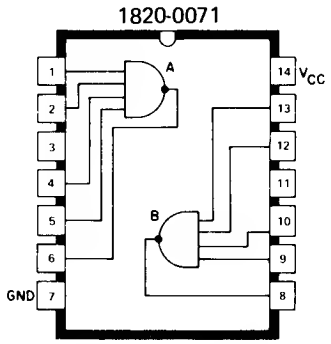

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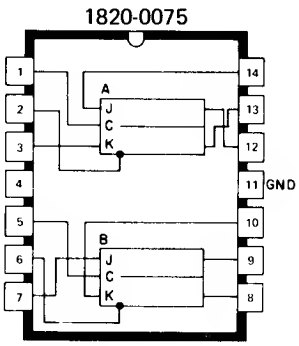

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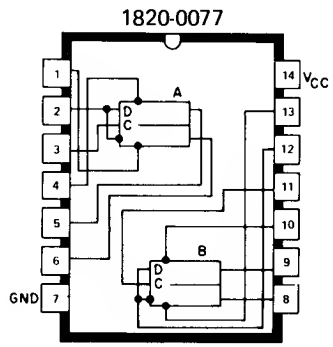

CHARACTERISTIC 8

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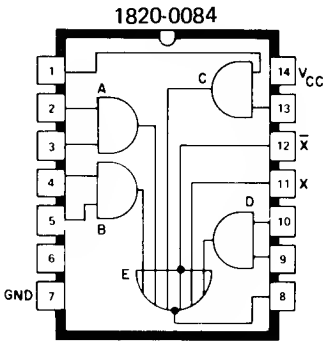

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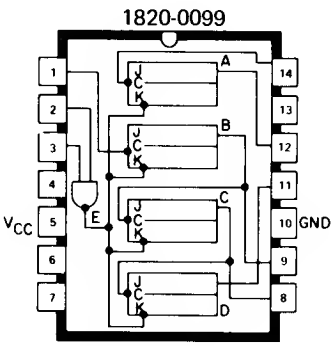

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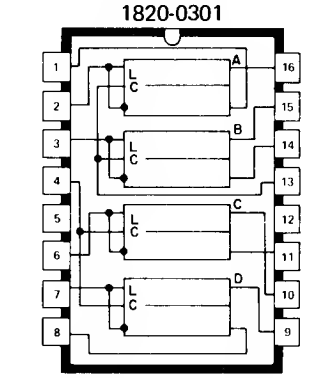

CHARACTERISTIC 9

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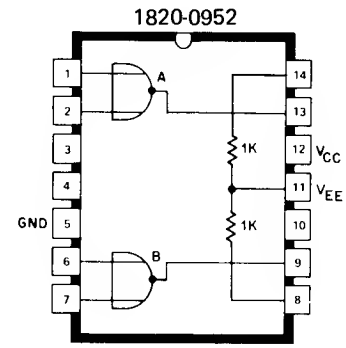

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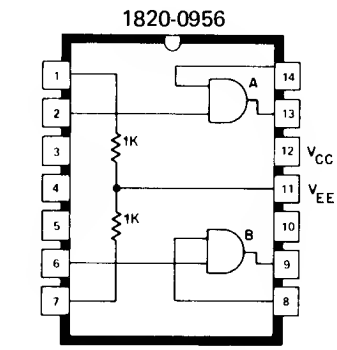


CHARACTERISTIC 17

2032-12

Figure 5-1. Integrated Circuit Pin Connections

Table 5-1. Integrated Circuit Input Levels, Output Levels, and Delay Times

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO 1 (NANOSEC)	TO 0 (NANOSEC)
2	+2.0	+0.8	+2.4	+0.4	Logic 1	29	15
7	+2.0	+0.8	+2.4	+0.4	Logic 1	50	50
8	+2.0	+0.8	+2.4	+0.4	Logic 1	35	50
9	+2.0	+0.8	+2.4	+0.4	Logic 1	40	25
15	+1.25	+0.5	+2.35	-0.36	Logic 0	14	12
17	+1.25	+0.5	+2.25	-0.36	Logic 0	18	18
29	+2.0*	+0.8†	+2.4	+0.4	Logic 1	125	135

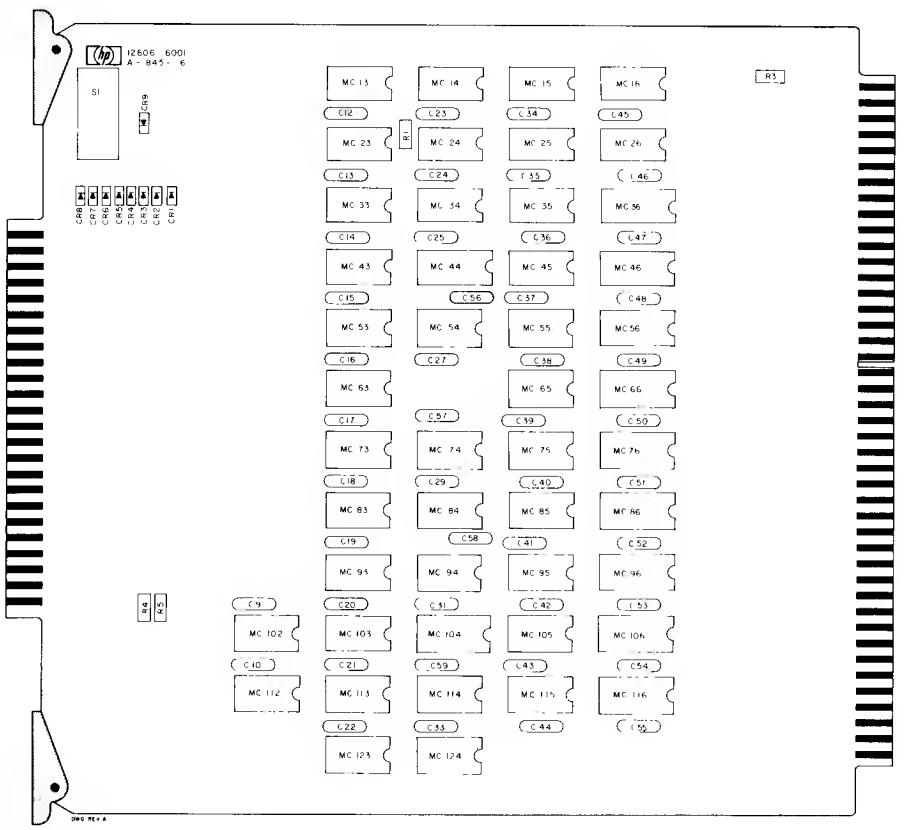
NOTES:

* +2.2V for pin 1

† +0.6V for pin 1

Table 5-2. Data Channel Interface Card (12606-6001), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C9,10, C12 thru C25,27 29,31, C33 thru C59	0160-2055	Capacitor, Fxd, Cer, 0.01 uf, +80-20%, 200 VDCW	56289	224P22402
CR1 thru CR8	1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG1088
CR9	1901-0460	Diode, Si, 3-Junction Stabistor	03508	STB523
MC13	1820-0069	Integrated Circuit, TTL	56289	USN7420A
MC14,84,123,124	1820-0071	Integrated Circuit, TTL	01295	SN4346
MC15,16,34,54,74,94,102, 112,114	1820-0054	Integrated Circuit, TTL	01295	SN4342
MC23	1820-0952	Integrated Circuit, CTL	07263	SL3455
MC24	1820-0075	Integrated Circuit, TTL	01295	SN4353
MC25,35,45,55,65,75,85,95, 105,115	1820-0956	Integrated Circuit, CTL	07263	SL3458
MC26	1820-0068	Integrated Circuit, TTL	56289	USN7410A
MC33,43,53,63,73,83,93, 103,113	1820-0077	Integrated Circuit, TTL	01295	SN4354
MC36,44,46,56,66,76,86,96, 104,106,116	1820-0301	Integrated Circuit, TTL	01295	SN4463
R1,2	0698-0082	Resistor, Fxd, Met Flm, 464 ohms, 1%, 1/8w	14674	C4 OBD
R3	0757-0280	Resistor, Fxd, Met Flm, 1k, 1%, 1/8w	14674	C4 OBD
R4,5	0698-3132	Resistor, Fxd, Flm, 261 ohms, 1%, 1/8w	28480	0698-3132
S1	3101-0932	Switch, Slide, DPDT, 0.5A, 125V, AC/DC	79727	GG350-0001



2032-13

Figure 5-2. Data Channel Interface Card (12606-6001), Part Location Diagram

Table 5-3. Data Channel Interface Card, 48-Pin Connector Signals

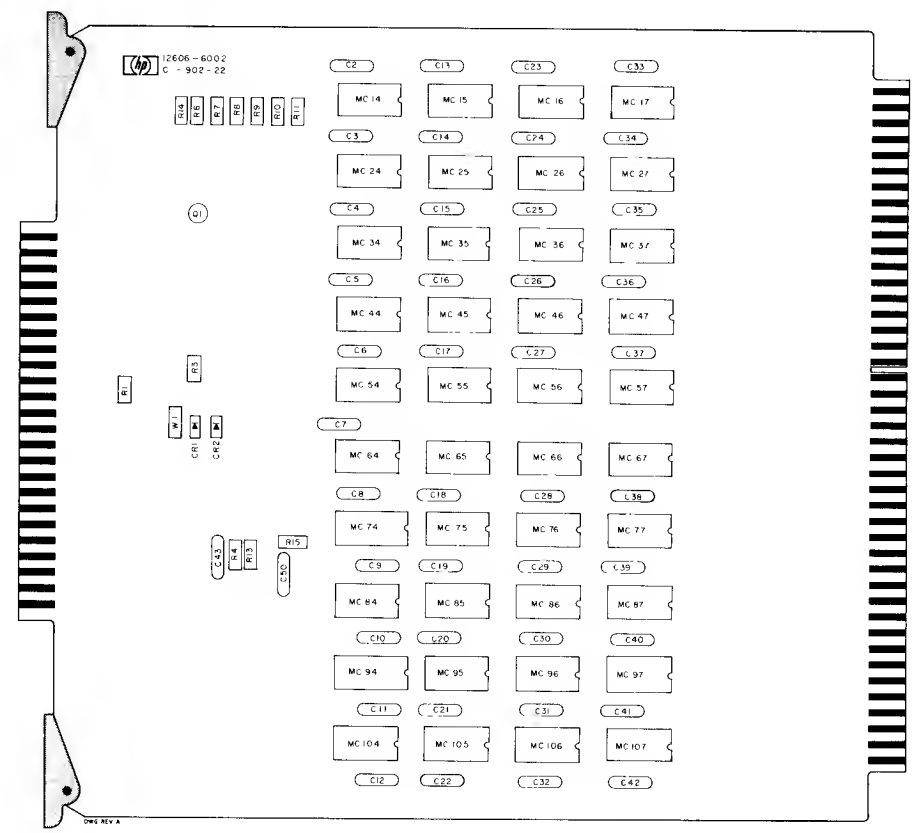
SIGNAL	DATA CARD PIN		CONNECTED TO:	
	SIGNAL	GROUND	SIGNAL	GROUND
$\overline{BC}$ (B) ("not" bit clock, buffered)	DAT-*R	–	CMD-*R	–
CB (Control Bit FF)	DAT-*W	–	CMD-*W	–
$\overline{CRA}$ ("not" clear RPE and ABS FFs)	DAT-*13	–	CMD-*13	–
$\overline{CRF}$ ("not" clear Run FF)	DAT-*Z	–	CMD-*Z	–
DI (Direction FF)	DAT-*T	–	CMD-*T	–
$\overline{DI}$ ("not" Direction FF)	DAT-*20	–	CMD-*20	–
DR (data read)	DAT-*23	DAT-*24	J10-P	J10-R
DW (data write)	DAT-*AA	DAT-*BB	J10-M	J10-N
$\overline{EWR}$ ("not" end-of-word, read)	DAT-*15	–	CMD-*15	–
$\overline{EWW}$ ("not" end-of-word, write)	DAT-*S	–	CMD-*S	–
$\overline{EWW}$ ("not" end-of-word, write)	DAT-*17	–	CMD-*17	–
RFW (ready for first word)	DAT-*U	–	CMD-*U	–
RP (Read Parity FF)	DAT-*V	–	CMD-*V	–
RUN	DAT-*14	–	CMD-*14	–
$\overline{STA}$ ("not" strobe track address)	DAT-*19	–	CMD-*19	–
TA0 (track address bit 0)	DAT-*1	DAT-*2	J10-a	J10-b
TA1 (track address bit 1)	DAT-*3	DAT-*B	J10-c	J10-d
TA2 (track address bit 2)	DAT-*4	DAT-*5	J10-e	J10-f
TA3 (track address bit 3)	DAT-*6	DAT-*E	J10-h	J10-j
TA4 (track address bit 4)	DAT-*7	DAT-*8	J10-k	J10-m
TA5 (track address bit 5)	DAT-*9	DAT-*J	J10-n	J10-p
TA6 (track address bit 6)	DAT-*10	DAT-*8	J10-r	J10-s
TA7 (track address bit 7)	DAT-*12	NC	NC	NC
$\overline{TP}$ ("not" track protect)	DAT-*16	–	CMD-*16	–
$\overline{WRD}$ ("not" Word FF)	DAT-*P	–	CMD-*P	–

NOTES:

"DAT-*" identifies a pin in the 48-pin connector for the data channel interface card.
"CMD-*" identifies a pin in the 48-pin connector for the command channel interface card.
"J10-" identifies a pin in J10 on the disc memory.
"NC" indicates no connection.
A dash for a ground return indicates that the common ground return between cards is used (pins 1, 2, 85, and 86 of the 86-pin connector). All signals transferred between the two interface cards use the common ground return. Each signal transferred to or from the disc uses a separate ground return, with the ground lead and signal lead forming a twisted pair.

Table 5-4. Command Channel Interface Card (12606-6002), Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C2 thru C42,50	0160-2055	Capacitor, Fxd, Cer, 0.01 uf, +80 -20%, 200 VDCW	56289	224P22402
C43	0150-0050	Capacitor, Fxd, Cer, 1000 pf, 600 VDCW	77630	OBD
CR1,2	1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG1088
MC14	1820-0071	Integrated Circuit, TTL	01295	SN4346
MC15,44,66,104	1820-0069	Integrated Circuit, TTL	56289	USN7420A
MC16,17,27,37,47,57,67,77,87, 97,107	1820-0956	Integrated Circuit, CTL	07263	SL3458
MC24,25,26,34,55,65	1820-0054	Integrated Circuit, TTL	01295	SN4342
MC35,36	1820-0077	Integrated Circuit, TTL	01295	SN4354
MC45,54,64	1820-0099	Integrated Circuit, TTL	01295	SN4462
MC46,56,84	1820-0068	Integrated Circuit, TTL	56289	USN7410A
MC74,94	1820-0301	Integrated Circuit, TTL	01295	SN4463
MC75,85,95,105	1820-0084	Integrated Circuit, TTL	01295	SN3449
MC76,86,96,106	1820-0075	Integrated Circuit, TTL	01295	SN4353
Q1	1854-0215	Transistor, Si, NPN	04713	SPS3611
R1	0757-0401	Resistor, Fxd, Met Flm, 100 ohms, 1%, 1/8w	14674	C4 OBD
R3	0698-0082	Resistor, Fxd, Met Flm, 464 ohms, 1%, 1/8w	14674	C4 OBD
R4, R6 thru R11,13	0698-3132	Resistor, Fxd, Flm, 261 ohms, 1%, 1/8w	28480	0698-3132
R14	0698-3445	Resistor, Fxd, Met Flm, 348 ohms, 1%, 1/8w	14674	C4 OBD
R15	0757-0280	Resistor, Fxd, Met Flm, 1k, 1%, 1/8w	14674	C4 OBD
W1	8159-0005	Jumper Wire	28480	8159-0005



2032-14

Figure 5-4. Command Channel Interface Card (12606-6002), Part Location Diagram

DATA CHANNEL INTERFACE CARD (12606-6001, REV 845)

TRACK ADDRESS REGISTER

TA0 FF MC104D
TA1 FF MC104C
TA2 FF MC104B
TA3 FF MC104A
TA4 FF MC44D
TA5 FF MC44C
TA6 FF MC44B
TA7 FF MC44A

MC112B MC112C MC112A MC112 MC102A MC102C MC102D MC102B MC84B

CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9

S1 TRACK PROTECT SWITCH +4.5V

*1 TA0 *3 TA1 *4 TA2 *6 TA3 *7 TA4 *9 TA5 *10 TA6 *12 TA7 *16 $\overline{TP}$ *19 $\overline{STA}$

A B C,D,E,F,G,H,I,J

GND PRH +4.5V -2V

C9 C10 C12 C13-C25 C27 C29 C31 C33 C34 C36 C38 C40 C42 C44 C45-C59

C35 C37 C39 C41 C43

PRL

SCM SCL IOGE(B) CLF EWR IOO DI STC CLC IOI RFW EWW CRS POPIO $\overline{DI}$ DR $\overline{RUN}$ $\overline{BC(B)}$

MC26B MC16A MC16C MC124A MC16D MC64A MC14B MC16B MC15C MC25A MC15A MC124B MC15B MC23A MC34C MC23B MC34D MC123A MC35B

MC25R1 MC25R2 MC35R1 R1 464 R2 464 R3 1K R4 261 R5 261 MC23R2 1K

*2 *5 *8 *11 *14 *17 *20 *23 *R *S *T *U

FLAG FF MC13A MC13B MC25B SRQ

CONTROL BIT FF MC15D MC14A *W CB *13 $\overline{CRA}$ *Z $\overline{CRF}$

RP FF MC33B *V RP

K L M N O P Q A B R

INPUT AND OUTPUT REGISTERS DATA SHIFT REGISTER

IOB016 IOB015 IOB014 IOB013 IOB012 IOB011 IOB010 IOB009 IOB008

I16 FF MC116A O16 FF MC116C O16 FF MC113A
I15 FF MC116B O15 FF MC116D O15 FF MC113B
I14 FF MC106A O14 FF MC106C O14 FF MC103A
I13 FF MC106B O13 FF MC106D O13 FF MC103B
I12 FF MC96A O12 FF MC96C O12 FF MC93A
I11 FF MC96B O11 FF MC96D D11 FF MC93B
I10 FF MC86A O10 FF MC86C O10 FF MC83A
I9 FF MC86B O9 FF MC86D O9 FF MC83B
I8 FF MC76A O8 FF MC76C O8 FF MC73A

MC115R2 MC115R1 MC105R2 MC105R1 MC95R2 MC95R1 MC85R2 MC85R1 MC75R2

MC114A MC115A MC114B MC115B MC114C MC105A MC114D MC105B MC94A MC95A MC94B MC95B MC94C MC85A MC94D MC85B MC74A

IOBI16 IOBI15 IOBI14 IOBI13 IOBI12 IOBI11 IOBI10 IOBI9

D,E,F,G,H,I,J O P M N L R Q S

NOTE:
CARD PINS DESIGNATED WITH AN ASTERISK PLUG INTO THE 48-PIN INTERFACE CONNECTOR, THOSE DESIGNATED WITHOUT PLUG INTO THE 86-PIN BACK PLANE CONNECTOR.

INPUT AND OUTPUT REGISTERS

IOB07 IOB06 IOB05 IOB04 IOB03 IOB02 IOB01 IOB00

I8 FF MC76A O8 FF MC76C
I7 FF MC76B O7 FF MC76D
I6 FF MC66A O6 FF MC66C
I5 FF MC66B O5 FF MC66D
I4 FF MC56A O4 FF MC56C
I3 FF MC56B O3 FF MC56D
I2 FF MC46A O2 FF MC46C
I1 FF MC46B O1 FF MC46D
I0 FF MC36A O0 FF MC36C

MC75R1 MC65R1 MC55R2 MC55R1 MC45R2 MC45R1 MC35R2

MC75A MC74B MC75B MC74C MC65A MC74D MC65B MC54A MC55A MC54B MC55B MC54C MC45A MC54D MC45B MC34A MC35A MC34B

*P $\overline{WRD}$ C O P M N

DWG REV B

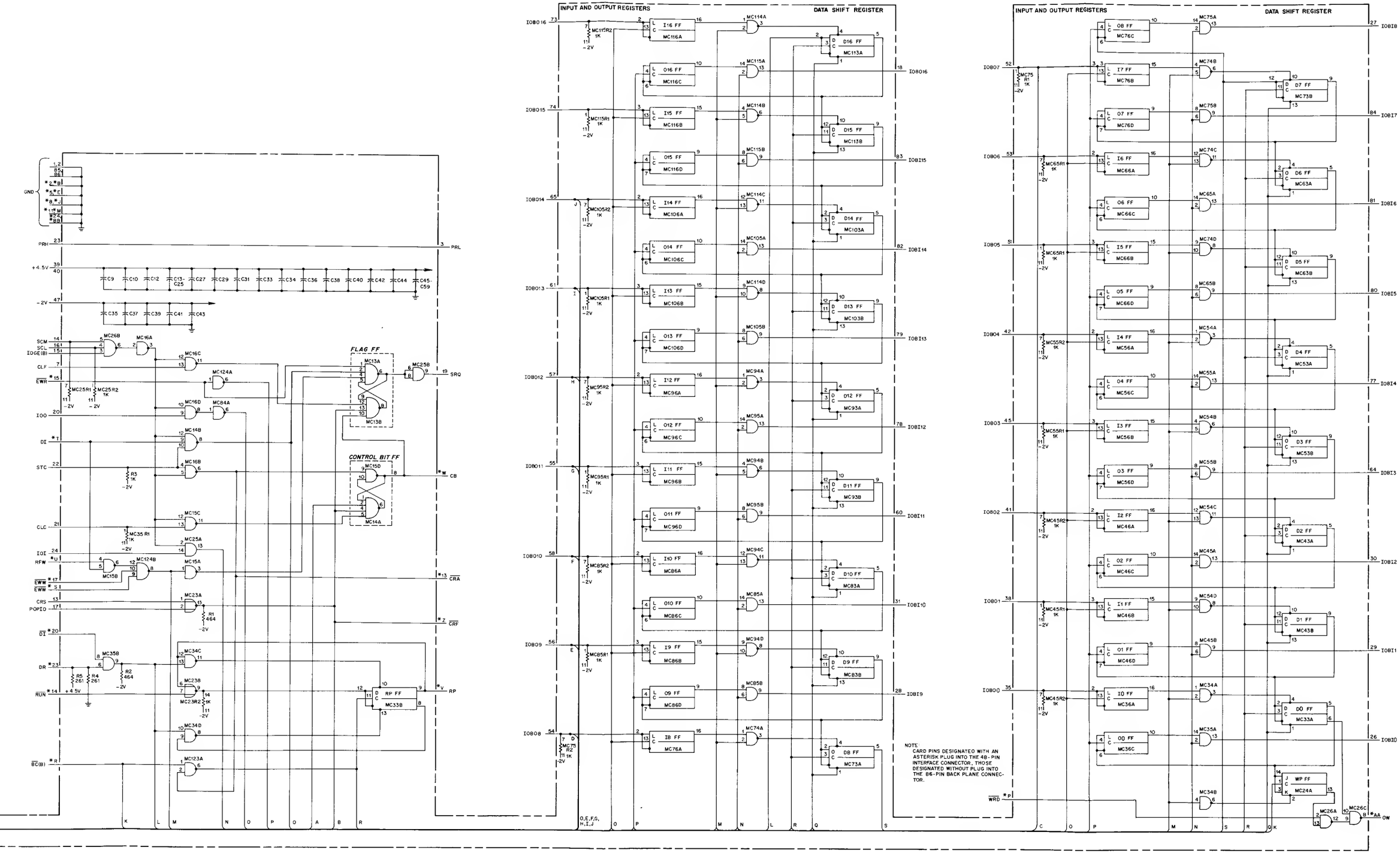


Figure 5-3. Data Channel Interface Card (12606-6001), Schematic Diagram

Table 5-5. Command Channel Interface Card, 48-Pin Connector Signals

SIGNAL	COMMAND CARD PIN		CONNECTED TO:	
	SIGNAL	GROUND	SIGNAL	GROUND
$\overline{\text{ACL}}$ ("not" AC voltage low)	CMD-*6	CMD-*5	J10-DD	J10-HH
$\overline{\text{BC}}$ ("not" bit clock)	CMD-*C	CMD-*B	J10-Y	J10-Z
$\overline{\text{BC}}$ (B) ("not" bit clock, buffered)	CMD-*R	–	DAT-*R	–
CB (Control Bit FF)	CMD-*W	–	DAT-*W	–
$\overline{\text{CRA}}$ ("not" clear RPE and ABS FFs)	CMD-*13	–	DAT-*13	–
$\overline{\text{CRF}}$ ("not" clear Run FF)	CMD-*Z	–	DAT-*Z	–
DI (Direction FF)	CMD-*T	–	DAT-*T	–
$\overline{\text{DI}}$ ("not" DI FF)	CMD-*20	–	DAT-*20	–
$\overline{\text{EWR}}$ ("not" end-of-word, read)	CMD-*15	–	DAT-*15	–
$\overline{\text{EWW}}$ ("not" end-of-word, write)	CMD-*S	–	DAT-*S	–
$\overline{\text{EWW}}$ ("not" end-of-word, write)	CMD-*17	–	DAT-*17	–
$\overline{\text{HC}}$ ("not" head change)	CMD-*H	CMD-*J	J10-K	J10-L
$\overline{\text{R}}$ ("not" read)	CMD-*4	CMD-*5	J10-U	J10-V
RFW (ready for first word)	CMD-*U	–	DAT-*U	–
$\overline{\text{RI}}$ ("not" read inhibit)	CMD-*F	CMD-*E	J10-H	J10-J
RP (Read Parity FF)	CMD-*V	–	DAT-*V	–
$\overline{\text{RUN}}$ ("not" Run FF)	CMD-*14	–	DAT-*14	–
$\overline{\text{RY}}$ ("not" disc ready)	CMD-*3	CMD-*2	J10-FF	J10-HH
$\overline{\text{SC}}$ ("not" sector clock pulse)	CMD-*A	CMD-*B	J10-W	J10-X
$\overline{\text{STA}}$ ("not" strobe track address)	CMD-*19	–	DAT-*19	–
$\overline{\text{TO}}$ ("not" track origin)	CMD-*1	CMD-*2	J10-E	J10-F
$\overline{\text{TP}}$ ("not" track protect)	CMD-*16	–	DAT-*16	–
$\overline{\text{W}}$ ("not" write)	CMD-*D	CMD-*E	J10-S	J10-T
$\overline{\text{WRD}}$ ("not" Word FF)	CMD-*P	–	DAT-*P	–

NOTES:

"DAT-*" identifies a pin in the 48-pin connector for the data channel interface card.
"CMD-*" identifies a pin in the 48-pin connector for the command channel interface card.
"J10-" identifies a pin in J10 on the disc memory.
A dash for a ground return indicates that the common ground return between cards is used (pins 1, 2, 85, and 86 of the 86-pin connector). All signals transferred between the two interface cards use the common ground return. Each signal transferred to or from the disc uses a separate ground return, with the ground lead and signal lead forming a twisted pair.

COMMAND CHANNEL INTERFACE CARD (12606-6002, REV 902)

IOBO-6 IOBO-5 IOBO-4 IOBO-3 IOBO-2 IOBO-1 IOBO-0

SC6 FF MC1D6B · S6 FF MC94 · SC5 FF MC106A · S5 FF MC94C · SC4 FF MC96B · S4 FF MC94D · SC3 FF MC96A · S3 FF MC74A · SC2 FF MC86B · S2 FF MC74B · SC1 FF MC86A · S1 FF MC74C · SCOFF MC76B · SO FF MC74D · SCP FF MC76A

MC105B MC105A MC105D MC105C MC1D5E · MC95B MC95A MC95D MC95C MC95E · MC85B MC85A MC85D MC85C MC85E · MC75B MC75A MC75D MC75C MC75E

+4.5V R8 261 R9 261 · C2-C6 C8-C33 C35 C37-C38 C40 C42 · C34 C36 C39 C41 · −2V · GND · +4.5V R15 1K

BC *C · RP *V · *2 *B · *5 *E · *8 *J · *11 *M · *24 *88 · 85,86 · ACL *6 · SC *A · CRA *13 · TD *1 · CLF 7 · PRH 23 · PRL 3 · IDI 24 · RY *3 · CB *W · SFC 5 · SCM 14 · SCL 16 · IDGE(B) 15 · SFS 25 · CRF *Z · IOO 20 · T3(B) 11

MC25A MC25B · MC54E MC64E MC348 · MC44A MC45E · MC24A MC24B MC24D MC14B MC24C · MC26C MC27A MC65A MC17A MC15A MC26D MC16A MC25C MC15B

R6 261 R7 261 · R10 261 R11 261 · MC37R1 1K · MC16R1 1K · R1 10D C7 · MC16R2 1K MC17R2 1K MC17R1 1K · +4.5V R14 348 · MC27R1 1K · MC37R2 1K · −2V

WORD COUNTER: WD0 FF MC54A · WD1 FF MC54B · WD2 FF MC54C · WD3 FF MC54D · WD4 FF MC64A · WD5 FF MC64B · EOS FF MC64C

BIT COUNTER: B0 FF MC45A · B1 FF MC45B · B2 FF MC45C · B3 FF MC45D · MC44B

STR FF MC35B · WRD FF MC35A · RPE FF MC36B

TOS FF: MC26A MC26B

SAC FF: MC55C MC66A · MC46A

ABS FF: MC84B MC34C · C50

RUN FF: MC56A MC66 · MC55D · MC56B MC56C · MC14A · MC34A · CR1 · CR2 · MC178 · MC278

I J K L I M

DWG REV B

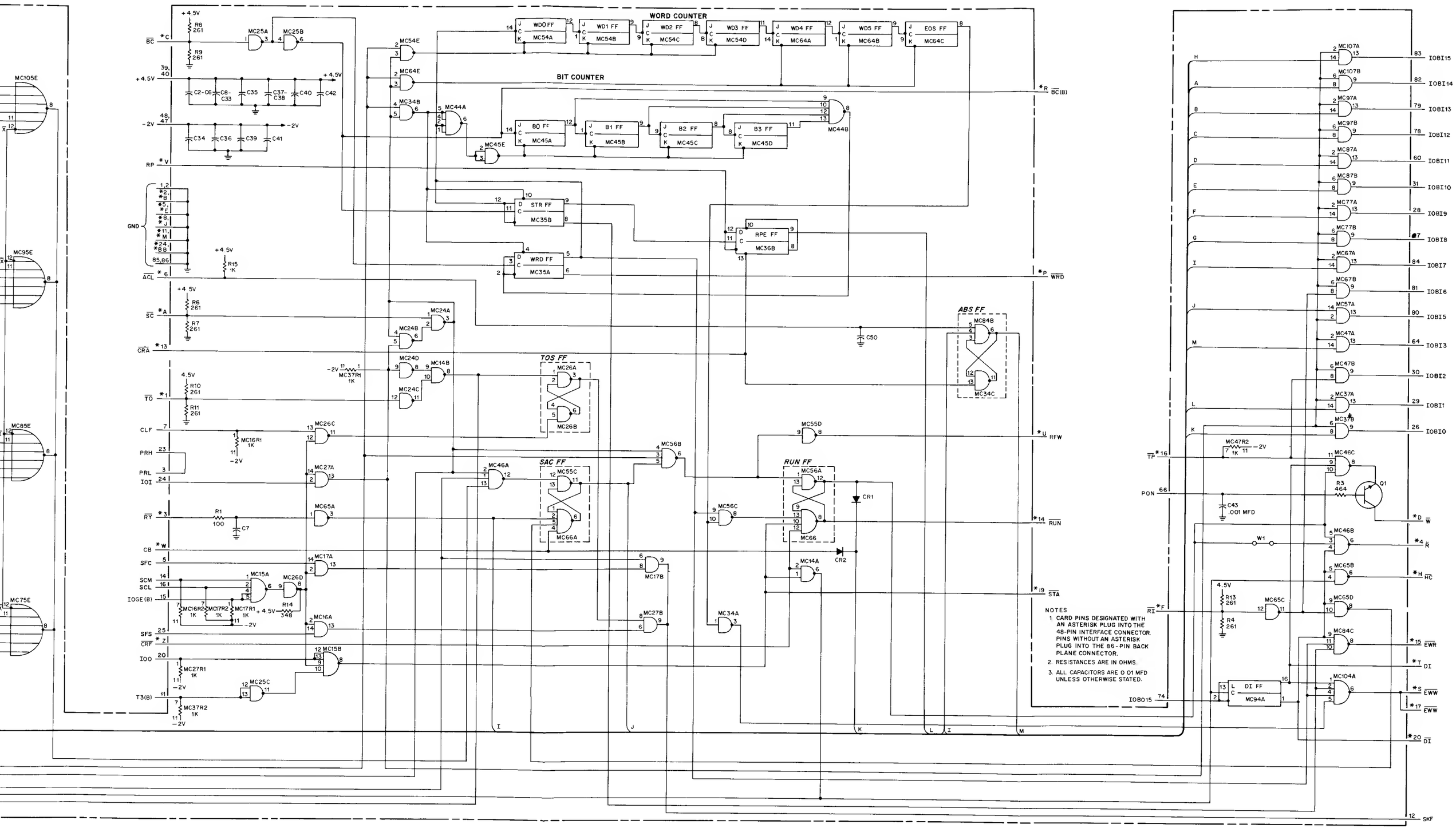


Figure 5-5. Command Channel Interface Card (12606-6002), Schematic Diagram

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section provides information for ordering replacement parts for the 12606B Disc Memory Interface Kit. Table 6-1 is a total-quantity listing of all replaceable parts in the kit.

6-3. Reference designation indexes (tables 5-2 and 5-4) and parts location diagrams (figures 5-2 and 5-4) for the data channel interface card and the command channel interface card are provided in section V of this manual adjacent to the logic diagram for each card.

6-4. Tables 5-2, 5-4, and 6-1 list the following information for each replaceable part:

a. Reference designation of the part (tables 5-2 and 5-4 only). Refer to table 6-2 for an explanation of abbreviations used in the REFERENCE DESIGNATION column.

b. Hewlett-Packard part number.

c. Description of the part. Refer to table 6-2 for an explanation of abbreviations used in the DESCRIPTION column.

d. A five digit code that corresponds to the manufacturer of the part. Refer to table 6-3 for a listing of the manufacturers that correspond to the codes.

e. Manufacturer's part number.

f. Total quantity (TQ) of each part used in the kit or assembly (table 6-1 only).

6-5. ORDERING INFORMATION.

6-6. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Identification of the instrument, kit, or assembly containing the part (refer to paragraph 1-9).

b. Hewlett-Packard part number for each part.

c. Description of each part.

d. Circuit reference designation (if applicable).

Table 6-1. Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TO
0150-0050	Capacitor, Fxd, Cer, 1000 pf, 600 VDCW	77630	OBD	1
0160-2055	Capacitor, Fxd, Cer, 0.01 uf, +80 -20%, 200 VDCW	56289	224P22402	88
0698-0082	Resistor, Fxd, Met Flm, 464 ohms, 1%, 1/8w	14674	C4 OBD	3
0698-3132	Resistor, Fxd, Flm, 261 ohms, 1%, 1/8w	28480	0698-3132	10
0698-3445	Resistor, Fxd, Met Flm, 348 ohms, 1%, 1/8w	14674	C4 OBD	1
0757-0280	Resistor, Fxd, Met Flm, 1k, 1%, 1/8w	14674	C4 OBD	2
0757-0401	Resistor, Fxd, Met Flm, 100 ohms, 1%, 1/8w	14674	C4 OBD	1
1820-0054	Integrated Circuit, TTL	01295	SN4342	15
1820-0068	Integrated Circuit, TTL	56289	USN7410A	4
1820-0069	Integrated Circuit, TTL	56289	USN7420A	5
1820-0071	Integrated Circuit, TTL	01295	SN4346	5
1820-0075	Integrated Circuit, TTL	01295	SN4353	5
1820-0077	Integrated Circuit, TTL	01295	SN4354	11
1820-0084	Integrated Circuit, TTL	01295	SN3449	4
1820-0099	Integrated Circuit, TTL	01295	SN4462	3
1820-0301	Integrated Circuit, TTL	01295	SN4463	13
1820-0952	Integrated Circuit, CTL	07263	SL3455	1
1820-0956	Integrated Circuit, CTL	07263	SL3458	21
1854-0215	Transistor, Si, NPN	04713	SPS3611	1
1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG1088	10
1901-0460	Diode, Si, 3-Junction Stabistor	03508	STB523	1
3101-0932	Switch, Slide, DPDT, 0.5A, 125V, AC/DC	79727	GG350-0001	1
8159-0005	Jumper Wire	28480	8159-0005	1
12606-6001	Data Channel Interface Card	28480	12606-6001	1
12606-6002	Command Channel Interface Card	28480	12606-6002	1
12606-6004	Interface Cable	28480	12606-6004	1
12606-90012	Operating and Service Manual	28480	12606-90012	1
20346C	Disc Diagnostic Tape	28480	20346C	1

HEWLETT PACKARD

MANUAL SUPPLEMENT

DIAGNOSTIC PROGRAM PROCEDURES

for

12606B

DISC MEMORY INTERFACE KIT

Note

Effective 1 July 1970 this preliminary manual supplement will be superseded by the HP 2770A/2771A Disc Memory Diagnostic Program Procedure (document part no. 12606-60013). The replacement text will be contained in the Manual of Diagnostics.

This supplement is part of, and should be attached to, the 12606B Drum Memory Interface Kit Operating and Service Manual.

12606-90012

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

Printed: MARCH 1970

TABLE OF CONTENTS

LIST OF TABLES

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This is a diagnostic test program. It contains a series of routines that test the reliability of all programmable features of a Hewlett-Packard 12606B Disc Memory Interface Kit and an HP 2770A/-001/-002/-003 or 2771A/-001/-002/-003 Disc Memory.

1-3. EQUIPMENT REQUIRED.

1-4. INSTRUMENTS:

a. Computer: HP computer with DMA option.

b. Teleprinter: HP 2752A or equivalent.

c. Punched Tape Reader: HP 2737A or equivalent.

d. Disc Memory: HP 2770A/-001/-002/-003 or 2771A/-001/-002/-003.

e. Disc Memory Power Supply: HP 2772A.

1-5. ACCESSORIES:

a. Teleprinter Interface Kit, HP 12531B.

b. Punched Tape Reader Interface Kit, HP 12532A.

c. Data Channel Interface Card, HP 12606-6001.

d. Command Channel Interface Card, HP 12606-6002.

e. Interface Cable, HP 12606-6004.

f. Main Power Cable, HP 8120-0078.

g. AC Power Interconnecting Cable, HP 02770-6003.

h. DC Power Interconnecting Cable, HP 02772-6003.

1-6. DIAGNOSTIC TAPE AND PROGRAMS.

Note

The part number of a program tape includes a suffix letter which identifies a particular revision of the tape. The first issue of a tape is identified by the letter A. Subsequent revisions are identified in alphabetical sequence as B, C, D, etc. If revision of a tape requires changes of associated documentation, an updating supplement for the documentation is supplied when the new tape is furnished. Always use the latest revision of a program tape, even if different from that specified in this manual, together with all updating documentation.

a. Diagnostic Tape, HP 20346C.

b. SIO Buffered Teleprinter Driver:

4K Memory — HP 20322A
8K Memory — HP 20323A
16K Memory — HP 20330B

c. SIO Buffered Punched Tape Reader Driver:

4K Memory — HP 20303A
8K Memory — HP 20306A
16K Memory — HP 20319A

SECTION II

PREPARATION

2-1. INTRODUCTION.

2-2. This section contains instructions for assembling a complete disc memory system of Hewlett-Packard components.

2-3. PRINTED CIRCUIT CARDS.

CAUTION

Turn off computer power before removing or inserting cards to prevent damage to cards, computer, or both.

2-4. PUNCHED TAPE READER CARD.

2-5. Insert punched tape reader interface card into an appropriate I/O slot in the computer.

2-6. TELEPRINTER CARD.

2-7. Insert teleprinter interface card into an appropriate I/O slot in the computer.

2-8. DISC CONTROLLER CARDS.

2-9. Insert the data channel and command channel interface cards into any two adjacent I/O slots with the 12606-6001 card in the higher priority location of the two. The track-protect switch will be located between the interface cards when they are correctly inserted. Interrupt priority to the disc controller interface cards is not necessary.

2-10. CABLES.

2-11. INTERFACE CABLE.

2-12. Connect the Interface Cable (12606-6004) from the interface cards to the disc memory.

CAUTION

Do not connect the AC Power Interconnecting Cable (02770-6003) to a power source other than the disc memory power supply (connector J2).

2-13. POWER INTERCONNECTING CABLES.

2-14. Connect the DC Power Interconnecting Cable (02772-6003) and the AC Power Interconnecting Cable (02770-6003) between the disc memory and the disc memory power supply.

2-15. MAIN POWER CABLE.

2-16. Connect the Main Power Cable (8120-0078) from the disc memory power supply to 115 volts ac.

2-17. DISC MEMORY.

2-18. Turn on the disc memory power supply and the computer.

2-19. Adjust the helium pressure to the disc memory as follows:

a. Read the low pressure gauge on the regulator, visible from the right side of the disc memory; pressure should be 1/4 psi to 1/2 psi, cold.

b. If necessary, adjust the helium pressure by bleeding; bleed by pulling down on the plunger valve located on the chassis, above and in front of the low pressure gauge. Helium pressure will rise as the disc warms up.

SECTION III

TEST INFORMATION

3-1. INTRODUCTION.

3-2. This section contains general instructions and tables to be used with the test procedures in Section IV.

3-3. NUMBER OF TRACKS.

3-4. Data is stored on the disc in parallel on double-circle tracks. Each track contains 90 (132 octal) sectors and each sector 64 words. Each word has 16 bits plus a parity bit. To determine the number of tracks in a given disc memory, note the HP Model number on the back of the top plate, next to the pressurized housing, and compare it to those listed in table 3-1.

Table 3-1. Table of Disc Memory Tracks

HP MODEL NUMBER	NUMBER OF TRACKS
2770A	32 (40 octal)
2770A-001/-002/-003	64 (100 octal)
2771A	64 (100 octal)
2771A-001/-002/-003	128 (200 octal)

3-5. DATA TRANSFER BLOCK SIZES.

3-6. Table 3-2 lists the capacity of various core memories to store data en bloc. This characteristic of a core memory limits the quantity of data that can be written into the disc memory or read out of it in a single block.

Table 3-2. Table of Core Memory Data Transfer Block Capacity

CORE MEMORY SIZE	DATA TRANSFER BLOCK SIZE
4096 (4K) 16 bit words	11 (13 octal) sectors or 704 words
8192 (8K) 16 bit words	74 (112 octal) sectors or 4,736 words
16,384 (16K) 16 bit words	90 (132 octal) sectors or 5,760 words

3-7. CORE REQUIREMENTS FOR TEST PROGRAM.

3-8. Table 3-3 lists the core locations that will be used by the diagnostic test program.

3-9. OCTAL NOTATION.

3-10. While this diagnostic test program is running, all numbers contained in input parameters or output messages are expressed in octal notation.

Table 3-3. Table of Core Requirements for Test Programs

CORE MEMORY SIZE	LOCATIONS
All Sizes	000100 — 001726
All Sizes	002000 — 005737
PLUS ONE OF THE FOLLOWING	
4096 (4K) 16 bit words	007235 — 007677
8192 (8K) 16 bit words	017235 — 017677
16,384 (16K) 16 bit words	037235 — 037677

3-11. LOOPING READ OR WRITE ROUTINES.

3-12. Since some errors may not appear until after the disc has been running for several minutes, both read and write routines should be set to loop for at least 10 minutes when conducting any test (see table 3-4). The status of both read and write routines is shown by indicator lights on the computer. Indicator lights 6 through 15 in the B-register remain on steadily during a write routine. Indicator lights 6 through 15 in the B-register blink on and off during a read routine.

Table 3-4. Table of Control Settings for Looping Routines

SWITCH REGISTER BIT SET TO LOGIC "1"	REACTION UNTIL SWITCH REGISTER BIT SET TO LOGIC "0"
Bit 2	Read routine loops
Bit 1	Write routine loops
Bit 0	Both read and write routines loop

3-13. VARIED TEST PATTERNS.

3-14. Several binary test patterns should be tried during the read or write routines; for example, all ones, all zeros, an even number of ones, an odd number of ones, etc. The total test running time should be at least 30 minutes.

3-15. EXECUTION MESSAGE SUPPRESSION.

3-16. During execution of the read or write routines, switch register bit 3 set to logic "1" suppresses all execution error messages except "DISC NOT READY".

3-17. READING OR WRITING BLOCKS.

3-18. If it is desirable to read or write selected blocks of tracks or sectors, they may be specified in the following manner:

T000-001, T020-007, T040-010, T070-002

3-19. The above statement would read or write the following octal track addresses:

000, 020 021 022 023 024 025 026, 040
041 042 043 044 045 046 047, 070 071

3-20. Sector block S020-004 would write the following sector addresses:

020 021 022 023

3-21. PARAMETER SPLIT BETWEEN LINES.

3-22. A virgule(/) is used to continue a statement on the next 72 column line. It must appear prior to or in column 72. No parameter may be split between two lines, as shown in the following example:

T000-001- - - - - - - - - - - - - - T060-/
001 etc.

3-23. If such a split is encountered, the following message is printed:

"WRITE PARAMETER INCOMPLETE".

3-24. The correct format for continuing a statement on the next line is as follows:

T000-001- - - - - - - - - - - - - - T060-001 /
T061-003 etc.

3-25. COUNTING ERRORS WITHOUT THE TELEPRINTER.

3-26. To run the diagnostic test program for long periods with the teleprinter off and still keep a record of accumulated word errors, it is only necessary to set switch register bits 0 and 3 to logic "1". Bit 0 set to logic "1" enables read and write routines to loop. Bit 3 set to logic "1" inhibits the teleprinter and enables each word error to increment an error counter, comprising memory locations 001700 and 001701. After 65,536 increments location 001700 overflows and each subsequent word error increments location 001701. When the total count of word errors is 131,072, the counter is reset and counting continues.

3-27. When switch register bits 0 and 3 are reset to logic "0", the teleprinter prints "BINARY TEST PATTERN?". The error counter (locations 001700 and 001701) must be read before entering a new binary test pattern. Entering a new pattern will reset the error counter.

3-28. RETURNING TO "BINARY TEST PATTERN?".

3-29. After the messages "DMA OCTAL CHANNEL #?" and "HIGH PRIORITY OCTAL ADDRESS?" have been initiated, address 002042 can be used at any time to return the program to the point where the teleprinter prints "BINARY TEST PATTERN?".

3-30. GLOSSARY OF DIAGNOSTIC MESSAGES.

3-31. "DISC NOT READY"

3-32. After this message is printed, the routine halts and allows the user to ready the disc memory for data transfer. If RUN is pressed before the disc memory is ready, the teleprinter will continue printing the message. This message usually indicates a malfunction of the "disc ready" status bit. This message has the same meaning for both the write and read routines.

3-33. "ERROR BUSY STATUS BIT DURING WR/RD"

3-34. After this message is printed, the routine does not halt and the current operations are completed normally. The "busy" status bit is checked just before the initiation of a write or a read operation for a "not busy" condition. If either condition is false at the appropriate time, this message is printed.

3-35. "WRITE (or READ) ABORT—TRACK"
020 (000-177)

3-36. This message indicates one or more of the following: a malfunction of disc power, overheating of the disc unit, helium pressure low, a power failure has occurred, or a write or read was attempted on either a protected or a nonexistent track address.

3-37. "WRITE (or READ) INTERRUPT MISSING"
"DMA WORD COUNT = " 167777

3-38. This message indicates that, after a write operation is initiated, no interrupt occurred within approximately 100 ms. By inspecting the DMA word count, the user can determine whether any words were transferred and, if so, how many prior to time-out. The DMA word count is output in 2s complement form. The routine does not halt after printing this message.

3-39. "READ PARITY ERROR"

3-40. This message indicates that a parity error occurred while reading a word.

3-41. "READ (or WRITE) SECTOR BUFFER OVERFLOWED"

3-42. This message occurs when more than 92 entries into the write or read sector buffer are specified for any series of "S" parameters.

3-43. "READ PARAMETER INCOMPLETE"

3-44. This message occurs if an illegal character is used in, or a character is missing from, any read parameter.

3-45. "WR/RD WORD COUNT EXCESSIVE"

3-46. This message occurs if a data transfer block size greater than available core memory is specified by single "S" parameter.

3-47. "IMPROPER CHARACTER IN WR/RD PARAMETER"

3-48. This message occurs when a character in a write or a read parameter is missing or has been replaced by an illegal character.

3-49. "CHARACTER IN OCTAL PARAMETER ILLEGAL"

3-50. This message occurs when any character other than numerals 0 through 7 is used in an octal parameter. One example of an illegal character is the symbol @.

3-51. "WR/RD PARAMETER EXCEEDS 72 CHARACTERS"

3-52. This message occurs when a line has exceeded 72 columns.

3-53. "WRITE PARAMETER INCOMPLETE"

3-54. This message occurs when a parameter entry has been split between two lines.

3-55. "BINARY PARAMETER EXCEEDS 72 CHARACTERS"

3-56. This message occurs when a binary test pattern parameter contains an excessive amount of leading blanks. This usually happens while using a punched tape reader input.

3-57. "ILLEGAL CHARACTER IN TEST PATTERN PARAM"

3-58. This message occurs when a binary test pattern parameter contains a syntax error.

3-59. SWITCH REGISTER CONTROL SETTINGS.

3-60. Table 3-5 lists the various switch register settings that control execution of the diagnostic test program.

Table 3-5. Table of Switch Register Control Settings

BIT NUMBER	LOGIC SETTING	REACTION
15	0	Input from teleprinter
	1	Input from punched tape reader
14	0	Normal sector buffer input
	1	Preset sector buffer input
11	0	Bypass or exit track address test
	1	Loop on track address test
3	0	Execute write/read test error printout
	1	Bypass all write/read test error printout
2	0	Normal execution of read test routine
	1	Loop on read test routine
1	0	Normal execution of write test routine
	1	Loop on write test routine
0	0	Normal execution of read/write test routine
	1	Loop on read/write test routine

SECTION IV

TEST PROCEDURE

4-1. ENABLING AND LOADING.

4-2. Start the diagnostic test procedure as follows:

a. Turn on power to the entire system.

b. Allow several minutes for the disc to reach full speed, then check the three lamps on the left side of the disc memory.

c. When all three lamps are out, load and configure the SIO buffered teleprinter driver and the SIO buffered punched tape reader driver tapes if necessary.

d. Load the diagnostic tape. When loading is completed, check for HLT 77B, 102077 (octal) in the T-register. If the T-register does not read 102077 (octal) reload the diagnostic tape and check again.

e. When the T-register reads 102077 (octal), turn on the teleprinter.

4-3. TRACK-PROTECT TEST.

4-4. Test the track-protect circuit as follows:

a. Set track-protect switch to the up position, away from the center of the card (PROTECTED). The switch is located on the Data Channel card (12606-6001). Load address 002000, set all switch register switches to "zero," press PRESET and RUN.

b. "DMA OCTAL CHANNEL # ?" will be printed by the teleprinter. The answer input should be a two digit number 06 or 07 followed by pressing RETURN and LINE FEED. If inputs other than these two are given, the program repeats the inquiry message and waits for a proper input.

c. "HIGH PRIORITY OCTAL DISC ADDRESS?" will be printed by the teleprinter. The answer input should be the I/O Select Code of the Data Channel card (12606-6001). Each answer input must be followed by pressing RETURN and LINE FEED. "NO. OF PROTECTED TRACKS —" followed by a three digit octal number, should be printed by the teleprinter to indicate the total number of protected tracks.

d. Press HALT. Set the track-protect switch to the down position, toward the center of the card (no tracks protected).

e. Load address 002000.

4-5. TRACK ADDRESS TEST.

4-6. This test routine checks all track heads for opens and shorts. It writes the self-address of each track, sector 000, and then reads each track, checking for self-address. The routine assumes the tracks start with 000 and end with the maximum number, in a sequential manner.

4-7. If switch register bit 11 is set to logic "0" before the program reaches this routine, when it does reach it the routine will be bypassed. If switch register bit 11 is set to logic "0" after entering the routine, the routine will be exited. Initialize this routine as follows:

a. Set switch register bit 11 to logic "1".

b. Press PRESET and RUN.

c. Enter the correct answer intputs in response to "DMA OCTAL CHANNEL #?" and "HIGH PRIORITY OCTAL DISC ADDRESS?" (see paragraph 4-4, "b" and "c").

4-8. The initial inquiry message printed by the teleprinter is:

"NO. OF TRACKS?"

4-9. The answer input should be a three-digit octal number representing the total number of tracks (see table 3-1), not the last track address.

4-10. If an error is encountered, a message similar to the following example is printed:

"TRACK ADDRESS ERROR
EXPECTED TRACK—006 ACTUAL TRACK—014"

4-11. The octal values in the example mean track 006 was addressed, but track 014 was actually read; or when writing track 014, it was actually written on track 006.

4-12. Switch register bit 11 may be set to logic "0" immediately after the routine is entered into, since one execution of the routine provides a sufficient test. When the routine is exited, the following message is printed:

"TRACK ADDRESS CHECK COMPLETE"

4-13. READ/WRITE TEST.

4-14. This is the main routine in the diagnostic test program. It writes and reads user-selected word patterns on any sector or group of sectors and on any track or group of

tracks. After reading word patterns from the disc, the routine compares them to the word patterns that were written. When errors are encountered, messages describing them are printed by the teleprinter. The user selects word pattern content and specifies write and read parameters in response to the following messages printed by the teleprinter: "BINARY TEST PATTERN?", "WRITE TRACKS?", "WRITE SECTORS?", "READ TRACKS?", and "READ SECTORS?".

4-15. The word patterns used in this routine are composed of 16-bit binary words in 64-word sector buffers. Any combination of sixteen logic "0s" and "1s" can be used in a word. A sector buffer can be formed in any of the following optional ways:

a. A 64-word series of one 16-bit word repeated.

b. A 64-word series of one 16-bit word and its complement repeated alternately.

c. A 64-word series of any combination of 16-bit words.

4-16. The first two 64-word sector buffers, option "a" and option "b", are written into core memory from the teleprinter keyboard. The third, option "c", is written into core memory from the switch register.

4-17. If switch register bit 15 is set to logic "1", the punched tape reader will input answers to read and write parameter requests (such as "WRITE TRACKS?"). Errors encountered on the tape can be correeted via the teleprinter as follows:

a. Set switch register bit 15 to logic "0".

b. After the diagnostic message is printed, press RUN.

c. Enter the corrected parameter from the teleprinter.

d. Set switch register bit 15 to logic "1".

e. Press RETURN or LINE FEED on the teleprinter.

4-18. The Read/Write Test routine starts by checking switch register bit 14. If bit 14 is a logic "0", the teleprinter prints the following initial message:

"BINARY TEST PATTERN?"

4-19. At this point the user can form either of two 64-word sector buffer options described in paragraph 4-15, option "a" or option "b". The answer input in response to this message is contained in an 18-character field, as shown in the following example:

11Ø011Ø011Ø011ØØCC

4-20. The first sixteen characters are any combination of logic "0s" and "1s". The last two characters can be either "Cs" or blanks. In the example, the first "C" (character 17) indicates every alternate word of the 64-word sector buffer will be the complement of the initial word in the sector buffer (option "b"). The second "C" (character 18) indicates every sector will be the complement of the preceding sector. If both characters 17 and 18 are blanks, one 16-bit word will be repeated 64 times (option "a") and all sectors will be the same. Any syntax error in the binary test pattern parameter causes the teleprinter to print the following message:

"ILLEGAL CHARACTER IN TEST PATTERN PARAM"

4-21. When the Read/Write Test routine starts, if switch register bit 14 is a logic "1", the computer halts. At this point the user can form the third 64-word sector buffer option described in paragraph 4-15, option "c", as follows:

a. Set in the switch register and load into core memory a 64-word series of any combination of 16-bit words.

b. After sixty-four switch register words are loaded into memory, press RUN twice. The routine will proceed to request write and read parameters.

4-22. After the sector buffer is formed, the teleprinter prints the following message:

"WRITE TRACKS?"

4-23. The answer input depends on the number of tracks in the disc memory (see table 3-1). It consists of the character "T" followed by two groups of three digits each. For example, T000-200. The character "T" identifies the instruction as a track location. The first three digits are the octal value of the starting track address (range 000-177). The second group of three digits is the octal value of the number of consecutive tracks to be written. The example, T000-200, would write 200 tracks (128 decimal) starting at track zero.

4-24. The next message printed by the teleprinter is the following:

"WRITE SECTORS?"

4-25. With a computer that has an 8K (8192 words) memory, one possible answer input is S000-100, S100-032. This will write sectors 0 through 77 octal, and then sectors 100 through 131. The character "S" identifies the instruction as a sector location. The first and second groups of three digits carry the same information as they do in the response to "WRITE TRACKS?". To cover the entire 132 sectors, the answer input must be made in two statements because the sector buffer can handle only 112 octal locations in one transfer. See table 3-2 for data transfer block capacities of other memory sizes.

4-26. The teleprinter next prints the following message:

"READ TRACKS?"

4-27. The answer input for this message is identical to the response to "WRITE TRACKS?". See paragraph 4-23.

4-28. The final read parameter message printed by the teleprinter is the following:

"READ SECTORS?"

4-29. The answer input for this message is identical to the response to "WRITE SECTORS?". See paragraph 4-25.

4-30. After a read operation is executed, a comparison of input data is made and any error conditions are printed in the following format:

"TRACK" ØØØ "SECTOR" ØØØ "WORD NO." ØØ "OUTPUT" ØØØØØØ "INPUT" ØØØØØ1

4-31. "TRACK" will range from 000 to 177, "SECTOR" from 000 to 131, and "WORD" from 00 to 77. "OUTPUT" is the octal equivalent of a 6-digit word output from the computer to the disc. "INPUT" is the octal equivalent of a 6-digit word input to the computer from the disc (error).

4-32. SECTOR TIMING TEST.

4-33. Write a pattern over the entire disc. Read the disc in overlapping blocks and sectors as in the following example of an overlapping test. (See paragraphs 3-18, 3-19, and 3-20 for further information.)

"BINARY TEST PATTERN?"
111ØØØØ1111ØØØØØ
"WRITE TRACKS?"
TØØØ-Ø4Ø
"WRITE SECTORS?"
SØØØ-1ØØ, S1ØØ-Ø32
"READ TRACKS?"
TØØØ-Ø4Ø, TØØØ-Ø2Ø, TØ2Ø-Ø2Ø, TØØ7-Ø23
"READ SECTORS?"
SØØØ-1ØØ, S1ØØ-Ø32, SØ11-1ØØ

4-34. POWER FAILURE TESTS.

4-35. Primary power to the disc memory should be turned off and back on during a read cycle and during a write cycle. When power is turned off during a read cycle, there must be no resulting errors. When power is turned off during a write cycle, the entire data transfer may have errors. This is the only time, however, during the entire diagnostic test program that errors are permissible. Every failure of primary power to the disc memory should result in the teleprinter printing one or more of the following: "DISC NOT READY", "WRITE ABORT-TRACK", "READ ABORT-TRACK", "WRITE INTERRUPT MISSING", "READ INTERRUPT MISSING".

4-36. POWER FAILURE, READ CYCLE.

4-37. To check the power failure circuits the binary test pattern must be identical for both the read and write cycles. Proceed with the test as follows:

a. On completion of the last binary test pattern check, set all switch register switches to logic "0". When the teleprinter prints "BINARY TEST PATTERN?", enter 11ØØ11ØØ11ØØ11ØØCC.

b. When the teleprinter prints "WRITE TRACKS?", enter the total number of tracks available (see paragraph 4-23).

c. When the teleprinter prints "WRITE SECTORS?", enter the total number of sectors (see paragraph 4-25).

d. After the write statements have been executed, when the teleprinter prints "READ TRACKS?", enter the same answer input as for "WRITE TRACKS?".

e. When the teleprinter prints "READ SECTORS?", set switch register bit 2 to logic "1" and enter the same answer input as for "WRITE SECTORS?".

f. While the read routine is looping, turn off the power switch on the disc memory power supply.

g. Wait for the teleprinter to print "DISC NOT READY", then turn on the power switch.

h. Allow the disc to reach full speed, then press RUN.

i. Wait 2 minutes, then set switch register bit 2 to logic "0".

4-38. POWER FAILURE, WRITE CYCLE.

4-39. To check the power failure circuits during a write cycle proceed as follows:

a. When the teleprinter prints "BINARY TEST PATTERN?", enter 11ØØ11ØØ11ØØ11ØØCC.

b. When the teleprinter prints "WRITE TRACKS?", enter one track address, for example, T050-001.

c. When the teleprinter prints "WRITE SECTORS?", set switch register bit 1 to logic "1" and enter one sector address, for example, S050-001.

d. While the write routine is looping on one track and one sector, turn off the power switch on the disc memory power supply.

e. With the computer halted, wait for the teleprinter to print "DISC NOT READY", then turn on the power switch and allow the disc to reach full speed.

f. Set switch register bit 1 to logic "0", load address 002042, then press PRESET and RUN.

g. Enter the binary test pattern: 11ØØ11ØØ11ØØ11ØØCC.

h. When the teleprinter prints "WRITE TRACKS?" and "WRITE SECTORS?", the answer input for both should be SPACE, RETURN, and LINE FEED. Do not enter a track or a sector address.

i. When the teleprinter prints "READ TRACKS?", enter the total number of tracks available (see paragraph 4-23).

j. When the teleprinter prints "READ SECTORS?", enter the total number of sectors available (see paragraph 4-25). Errors must be confined to a chosen track and sector, for example, Track 50, Sector 50.